

Oct. 2025



SCC08GS03G2F1C-32AA

**260-Pin DDR4 Unbuffered SODIMM (X64, noECC)
EU RoHS Compliant**

Data Sheet

Rev. A

| Revision History | | |
|------------------|----------|----------------------------------------------|
| Date | Revision | Subjects (major changes since last revision) |
| 2025-10-09 | A | Initial Release |

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1 Overview

This chapter gives an overview of the 260-pin DDR4 Unbuffered SODIMM product family and describes its main characteristics.

1.1 Features

- 260-Pin PC4-3200 DDR4 SODIMM
- Frequency/CAS latency:
0.625ns @ CL = 22 (DDR4-3200)
- VDD = 1.2V(1.14V~1.26V)
- VPP = 2.5V(2.375V~2.75V)
- VDDSPD = 2.25V~3.6V
- Programmable CAS latency 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22 and 24 supported
- Programmable additive latency 0, CL-1, and CL-2 supported (x4/x8 only)
- Programmable CAS Write latency (CWL) = 9, 10, 11, 12, 14, 16, 18, 20
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- Data bus inversion (DBI) for data bus
- Fly-by topology
- Terminated control command and address bus
- BL switch on the fly
- 16 internal banks; 4 groups of 4 banks each
- Nominal and dynamic on-die termination (ODT) for strobe, and mask signals
- Low-power auto self refresh (LPASR)
- On-die VREFDQ generation and calibration
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Gold edge contacts
- Halogen-free
- Average Refresh Cycle (Tcase of 0 °C ~ 95 °C)
 - 7.8 μs at 0 °C ~ 85 °C
 - 3.9 μs at 85 °C ~ 95 °C

Table 1 - Module Performance Table

| UniC Speed Code | | -3200AA | Unit | Note |
|-------------------------|-------|----------|-----------------|------|
| DRAM Speed Grade | DDR4 | -3200 | MT/s | |
| CAS-RCD-RP latencies | | 22-22-22 | t _{CK} | |
| Min. RAS-CAS-Delay | 13.75 | 13.75 | ns | |
| Min. Row Precharge Time | 13.75 | 13.75 | ns | |
| Min. Row Active Time | 32 | 32 | ns | |
| Min. Row Cycle Time | 45.75 | 45.75 | ns | |

1.2 Description

The UnilC 8GB module family is DDR4 Unbuffered SODIMM with 30mm height based on DDR4 technology. DIMMs are intended for mounting into 260-pin connector sockets.

The memory array is designed with 8 Gbit Double-Data- Rate-Four (DDR4) Synchronous DRAMs. Decoupling capacitors are mounted on the PCB board. The DIMMs feature serial presence detect based on a serial E²PROM device using the 2-pin I²C protocol.



Table 2 - Ordering Information

| Product Type | Compliance Code ¹⁾ | Description | SDRAM Technology |
|---------------------|-------------------------------|-------------|------------------|
| SCC08GS03G2F1C-32AA | 8GB 1R×8 PC4-3200S-22-22-22 | 1 Rank | 8Gbit (×8) |

1) This describes the speed grade, for example "PC4-3200S-22-22-22" where 3200 means DIMM modules with 3200MT/s data rate and "22-22-22" means Column Address Strobe (CAS) latency=22, Row Column Delay (RCD) latency = 22 and Row Precharge (RP) latency = 22.

Table 3 - Address Format

| | |
|--------------------------------------|---------------|
| DIMM Density | 8GB(1Rx8,X64) |
| Row address | 128K A[15:0] |
| Column address | 1K A[9:0] |
| Device bank group address | 4 BG[1:0] |
| Device bank address per group | 4 BA[1:0] |
| Device configuration | 8Gb(1Gx8) |
| Module rank address | 1 CS_n[0] |
| Device Quantity | 8 |

2 Pin Configurations

2.1 Pin Configurations

The pin configuration of the 260-Pin DDR4 Unbuffered SODIMM is listed by function in [Table 4](#) (260 pins).

Table 4 - Pin Configuration SODIMM (260 pin)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|----------------------------------------|-----|----------------------------------------|-----|-------------------------|-----|--------------------------|-----|----------------------------------------------|-----|----------------------------------------------|
| 1 | VSS | 2 | VSS | 97 | DQS8 _t NC | 98 | VSS | 193 | VSS | 194 | DQ41 |
| 3 | DQ5 | 4 | DQ4 | 99 | VSS | 100 | CB6 /NC | 195 | DQ40 | 196 | VSS |
| 5 | VSS | 6 | VSS | 101 | CB2,NC | 102 | VSS | 197 | VSS | 198 | DQS5 _c NC |
| 7 | DQ1 | 8 | DQ0 | 103 | VSS | 104 | CB7,NC | 199 | DM5 _n /DBI5 _n NC | 200 | DQS5 _t NC |
| 9 | VSS | 10 | VSS | 105 | CB3 /NC | 106 | VSS | 201 | VSS | 202 | VSS |
| 11 | DQS0 _c | 12 | DM0 _n /DBI0 _n | 107 | VSS | 108 | RESET _n | 203 | DQ46 | 204 | DQ47 |
| 13 | DQS0 _t | 14 | VSS | 109 | CKE0 | 110 | CKE1 | 205 | VSS | 206 | VSS |
| 15 | VSS | 16 | DQ6 | 111 | VDD | 112 | VDD | 207 | DQ42 | 208 | DQ43 |
| 17 | DQ7 | 18 | VSS | 113 | BG1 | 114 | ACT _n | 209 | VSS | 210 | VSS |
| 19 | VSS | 20 | DQ2 | 115 | BG0 | 116 | ALERT _n | 211 | DQ52 | 212 | DQ53 |
| 21 | DQ3 | 22 | VSS | 117 | VDD | 118 | VDD | 213 | VSS | 214 | VSS |
| 23 | VSS | 24 | DQ12 | 119 | A12 | 120 | A11 | 215 | DQ49 | 216 | DQ48 |
| 25 | DQ13 | 26 | VSS | 121 | A9 | 122 | A7 | 217 | VSS | 218 | VSS |
| 27 | VSS | 28 | DQ8 | 123 | VDD | 124 | VDD | 219 | DQS6 _c NC | 220 | DM6 _n /DBI6 _n NC |
| 29 | DQ9 | 30 | VSS | 125 | A8 | 126 | A5 | 221 | DQS6 _t NC | 222 | VSS |
| 31 | VSS | 32 | DQS1 _c | 127 | A6 | 128 | A4 | 223 | VSS | 224 | DQ54 |
| 33 | DM1 _n /DBI1 _n | 34 | DQS1 _t | 129 | VDD | 130 | VDD | 225 | DQ55 | 226 | VSS |
| 35 | VSS | 36 | VSS | 131 | A3 | 132 | A2 | 227 | VSS | 228 | DQ50 |
| 37 | DQ15 | 38 | DQ14 | 133 | A1 | 134 | EVENT _n | 229 | DQ51 | 230 | VSS |
| 39 | VSS | 40 | VSS | 135 | VDD | 136 | VDD | 231 | VSS | 232 | DQ60 |
| 41 | DQ10 | 42 | DQ11 | 137 | CK0 _t | 138 | CK1 _t | 233 | DQ61 | 234 | VSS |
| 43 | VSS | 44 | VSS | 139 | CK0 _c | 140 | CK1 _c | 235 | VSS | 236 | DQ57 |
| 45 | DQ21 | 46 | DQ20 | 141 | VDD | 142 | VDD | 237 | DQ56 | 238 | VSS |
| 47 | VSS | 48 | VSS | 143 | Parity | 144 | A0 | 239 | VSS | 240 | DQS7 _c NC |
| 49 | DQ17 | 50 | DQ16 | 145 | BA1 | 146 | A10/AP | 241 | DM7 _n /DBI7 _n NC | 242 | DQS7 _t NC |
| 51 | VSS | 52 | VSS | 147 | VDD | 148 | VDD | 243 | VSS | 244 | VSS |
| 53 | DQS2 _c | 54 | DM2 _n /DBI2 _n | 149 | CS0 _n | 150 | BA0 | 245 | DQ62 | 246 | DQ63 |
| 55 | DQS2 _t | 56 | VSS | 151 | A14 /WE _n | 152 | A16 /RAS _n | 247 | VSS | 248 | VSS |
| 57 | VSS | 58 | DQ22 | 153 | VDD | 154 | VDD | 249 | DQ58 | 250 | DQ59 |

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|------------------|-----|------------------------|-----|---------------------|-----|------------------------|-----|--------|-----|------|
| 59 | DQ23 | 60 | VSS | 155 | ODT0 | 156 | A15 CAS_n/ | 251 | VSS | 252 | VSS |
| 61 | VSS | 62 | DQ18 | 157 | CS1_n | 158 | A13 | 253 | SCL | 254 | SDA |
| 63 | DQ19 | 64 | VSS | 159 | VDD | 160 | VDD | 255 | VDDSPD | 256 | SA0 |
| 65 | VSS | 66 | DQ28 | 161 | ODT1 | 162 | C0 /CS2_n /NC | 257 | VPP | 258 | Vtt |
| 67 | DQ29 | 68 | VSS | 163 | VDD | 164 | VREFCA | 259 | VPP | 260 | SA1 |
| 69 | VSS | 70 | DQ24 | 165 | C1 /CS3_n /NC | 166 | SA2 | | | | |
| 71 | DQ25 | 72 | VSS | 167 | VSS | 168 | VSS | | | | |
| 73 | VSS | 74 | DQS3_c | 169 | DQ37 | 170 | DQ36 | | | | |
| 75 | DM3_n /DBI3_n | 76 | DQS3_t | 171 | VSS | 172 | VSS | | | | |
| 77 | VSS | 78 | VSS | 173 | DQ33 | 174 | DQ32 | | | | |
| 79 | DQ30 | 80 | DQ31 | 175 | VSS | 176 | VSS | | | | |
| 81 | VSS | 82 | VSS | 177 | DQS4_c NC | 178 | DM4_n /DBI4_n NC | | | | |
| 83 | DQ26 | 84 | DQ27 | 179 | DQS4_t NC | 180 | VSS | | | | |
| 85 | VSS | 86 | VSS | 181 | VSS | 182 | DQ39 | | | | |
| 87 | CB5 /NC | 88 | CB4 /NC | 183 | DQ38 | 184 | VSS | | | | |
| 89 | VSS | 90 | VSS | 185 | VSS | 186 | DQ35 | | | | |
| 91 | CB1 /NC | 92 | CB0 /NC | 187 | DQ34 | 188 | VSS | | | | |
| 93 | VSS | 94 | VSS | 189 | VSS | 190 | DQ45 | | | | |
| 95 | DQS8_c NC | 96 | DM8_n /DBI8_n NC | 191 | DQ44 | 192 | VSS | | | | |

2.2 Pin Descriptions

Table 5 - Pin Descriptions

| Symbol | Type | Function |
|--------------------------------------|-------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CKx_t, CKx_c, | Input | Clock: CK_t and CK_c are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK_t and negative edge of CK_c. |
| CKEx | Input | Clock Enable: CKE HIGH activates and CKE LOW deactivates internal clock signals and device input buffers and output drivers. Taking CKE LOW provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for Self-Refresh exit. After VREFCA and Internal DQ Vref have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK_t, CK_c, ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh. |
| CSx_n | Input | Chip Select: All commands are masked when CS-n is registered HIGH. CS_n provides for external Rank selection. CS_n is considered part of the command code. |
| Cx | Input | Chip ID : Chip ID is only used for 3DS for 2,4,8 high stack via TSV to select each slice of stacked component. Chip ID is considered part of the command code. |
| ODTx | Input | On Die Termination: ODT (registered HIGH) enables RTT_NOM termination resistance internal to the DDR4 SDRAM. When enabled, ODT is only applied to each DQ, DQS_t, DQS_c, TDQS_t and TDQS_c signal. The ODT pin will be ignored if MR1 is programmed to disable RTT_NOM. |
| ACT_n | Input | Activation Command Input: ACT_n defines the Activation command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15 and WE_n/A14 will be considered as Row Address A16, A15 and A14 |
| RAS_n/A16. CAS_n/A15. WE_n/A14 | Input | Command Inputs: RAS_n/A16, CAS_n/A15 and WE_n/A14 (along with CS_n) define the command being entered. Those pins have multi function. For example, for activation with ACT_n Low, these are Addresses like A16, A15 and A14 but for non-activation command with ACT_n High, these are Command pins for Read, Write and other command defined in command truth table |
| BGx | Input | Bank Group Inputs: BG0 - BG1 define which bank group an Active, Read, Write or Precharge command is being applied. BG0 also determines which mode register is to be accessed during a MRS cycle. |
| BAx | Input | Bank Address Inputs: BA0 - BA1 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines which mode register is to be accessed during a MRS cycle. |
| Ax | Input | Address Inputs: Provide the row address for ACTIVATE Commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. A10/AP, A12/BC_n, RAS_n/A16, CAS_n/A15 and WE_n/A14 have additional functions. See other rows. The address inputs also provide the op-code during Mode Register Set commands. A17 is only defined for 16 Gb x4 SDRAM configurations. |
| A10 / AP | Input | Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses. |

| Symbol | Type | Function |
|--------------------------------------------------------------------|------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A12/BC_n | Input | Burst Chop: A12/BC_n is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details. |
| Parity | Input | Command and Address Parity Input: DDR4 Supports Even Parity check in SDRAMs with MR setting. Once it's enabled via Register in MR5, then SDRAM calculates Parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG0-BG1, BA0-BA1, A17-A0. Input parity should be maintained at the rising edge of the clock and at the same time with command & address with CS_n LOW |
| SAX | Input | Serial address inputs: Used to configure the temperature sensor/SPD EEPROM address range on the I2C bus. |
| SCL | Input | Serial clock for temperature sensor/SPD EEPROM: Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the I2C bus. |
| RESET_n | CMOS Input | Active Low Asynchronous Reset: Reset is active when RESET_n is LOW, and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. |
| DQx, CBx | I/O | Data Input/ Output: Bi-directional data bus. If CRC is enabled via Mode register then CRC code is added at the end of Data Burst. Any DQ from DQ0-DQ3 may indicate the internal Vref level during test via Mode Register Setting MR4 A4=High. Refer to vendor specific data sheets to determine which DQ is used. |
| DQSx_t-DQSx_c | I/O | Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS_t is paired with differential signals DQS_c, respectively, to provide differential pair signaling to the system during reads and writes. DDR4 SDRAM supports differential data strobe only and does not support single-ended. |
| DM_n/DBI_n/ TDQS_t (DMU_n, DBIU_n), (DML_n/ DBIL_n) | I/O | Input data mask and data bus inversion: DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/ output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs). |
| SDA | I/O | Serial Data: Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device. |
| ALERT_n | Output | Alert: It has multi functions such as CRC error flag, Command and Address Parity error flag as Output signal. If there is error in CRC, then ALERT_n goes LOW for the period time interval and goes back HIGH. If there is error in Command Address Parity Check, then ALERT_n goes LOW for relatively long period until ongoing SDRAM internal recovery transaction is complete. During Connectivity Test mode this pin functions as an input. |
| EVENT_n | Output | Temperature event: The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors. |

| Symbol | Type | Function |
|---------------------------------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TDQS_t TDQS_c (x8 DRAM-based RDIMM only) | Output | Termination data strobe: When enabled via the mode register, the DRAM device enables the same RTT termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component datasheet (TDQS_t and TDQS_c are not valid for UDIMMs). |
| VDD | Supply | Module power supply: 1.2V (TYP). |
| VPP | Supply | DRAM activating power supply: 2.5V -0.125V / +0.250V. |
| VREFCA | Supply | Reference voltage for control, command, and address pins. |
| VSS | Supply | Ground. |
| VTT | Supply | Power supply for termination of address, command, and control VDD/2. |
| VDDSPD | Supply | Power supply used to power the I2C bus for SPD. |
| RFU | - | Reserved for Future Use: No on DIMM electrical connection is present |
| NC | - | No Connect: No on DIMM electrical connection is present |

3 General Description

3.1 General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with 2 or 4 internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM have 4 internal bank groups consisting of 4 memory banks each, providing a total of 16 banks. Sixteen-bit-wide DDR4 SDRAM has 2 internal bank groups consisting of 4 memory banks each, providing a total of 8 banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8n-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding n-bit wide, one-half-clock-cycle data transfers at the I/O pins.

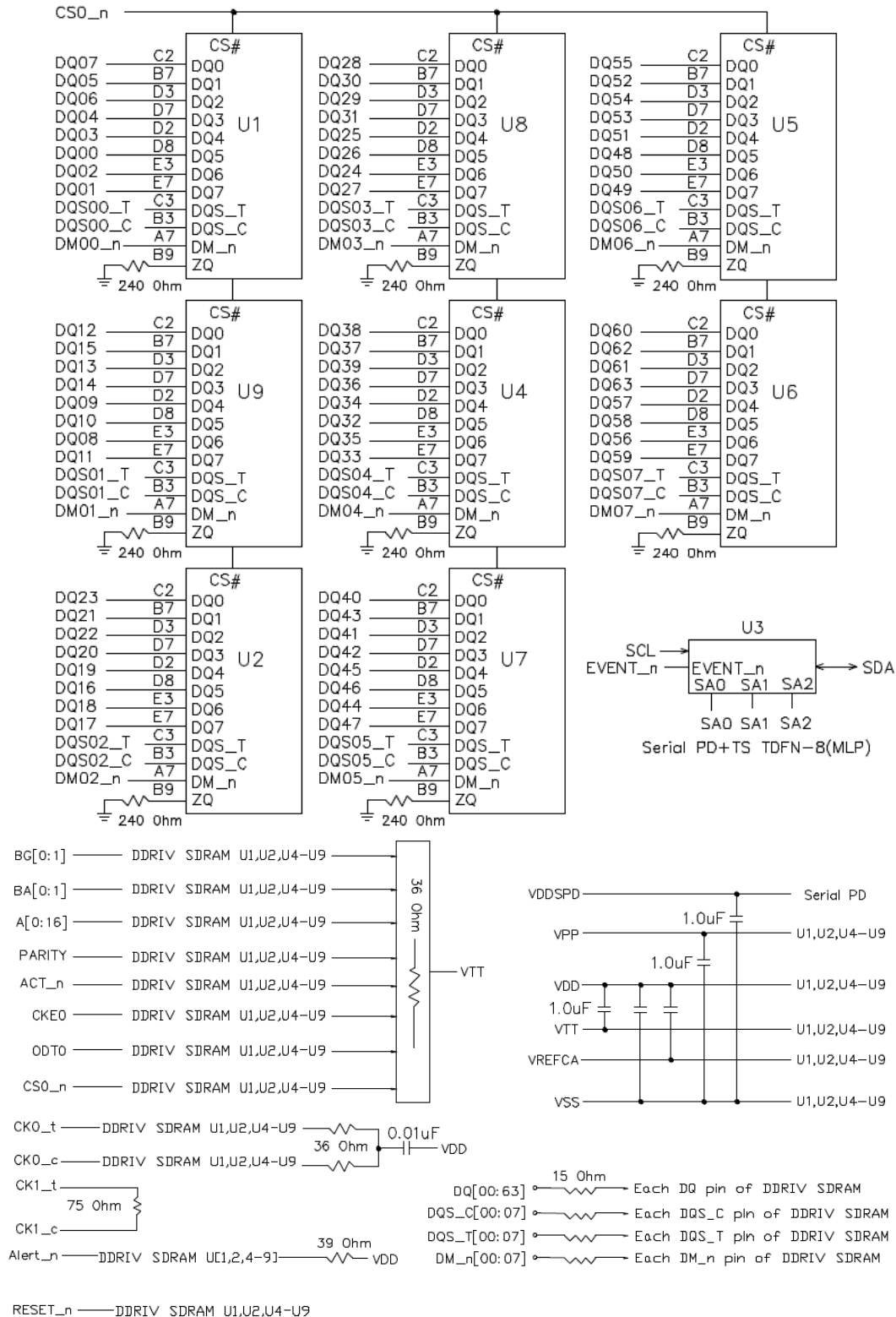
DDR4 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

3.2 Serial Presence-Detect EEPROM Operation

DDR4 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 512-byte EEPROM. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I2C bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to VSS, permanently disabling hardware write protection.

3.3 Function Block Diagram

Figure 1 - Function Block Diagram_SCC08GS03G2F1C-32AA



3.4 DQ Map

Table 6 - DQ Map_SCC08GS03G2F1C-32AA

| Module Pin NO. | Module DQ | Damping RES. | IC NO. | IC DQ | Module Pin NO. | Module DQ | Damping RES. | IC NO. | IC DQ |
|----------------|-----------|--------------|--------|-------|----------------|-----------|--------------|--------|-------|
| 8 | 0 | R98 | U1 | 5 | 28 | 8 | R93 | U9 | 6 |
| 7 | 1 | R6 | | 7 | 29 | 9 | R12 | | 4 |
| 20 | 2 | R95 | | 6 | 41 | 10 | R15 | | 5 |
| 21 | 3 | R10 | | 4 | 42 | 11 | R89 | | 7 |
| 4 | 4 | R199 | | 3 | 24 | 12 | R94 | | 0 |
| 3 | 5 | R5 | | 1 | 25 | 13 | R11 | | 2 |
| 16 | 6 | R96 | | 2 | 38 | 14 | R90 | | 3 |
| 17 | 7 | R9 | | 0 | 37 | 15 | R14 | | 1 |
| 50 | 16 | R87 | U2 | 5 | 70 | 24 | R82 | U8 | 6 |
| 49 | 17 | R17 | | 7 | 71 | 25 | R23 | | 4 |
| 62 | 18 | R84 | | 6 | 83 | 26 | R26 | | 5 |
| 63 | 19 | R21 | | 4 | 84 | 27 | R78 | | 7 |
| 46 | 20 | R88 | | 3 ^ | 66 | 28 | R83 | | 0 |
| 45 | 21 | R16 | | 1 | 67 | 29 | R22 | | 2 |
| 58 | 22 | R85 | | 2 | 79 | 30 | R25 | | 1 |
| 59 | 23 | R20 | | 0 | 80 | 31 | R79 | | 3 |
| 174 | 32 | R75 | U4 | 5 | 195 | 40 | R34 | U7 | 0 |
| 173 | 33 | R28 | | 7 | 194 | 41 | R70 | | 2 |
| 187 | 34 | R32 | | 4 | 207 | 42 | R37 | | 3 |
| 186 | 35 | R72 | | 6 | 208 | 43 | R66 | | 1 |
| 170 | 36 | R76 | | 3 | 191 | 44 | R33 | | 6 |
| 169 | 37 | R27 | | 1 | 190 | 45 | R71 | | 4 |
| 183 | 38 | R31 | | 0 | 203 | 46 | R36 | | 5 |
| 182 | 39 | R73 | | 2 | 204 | 47 | R67 | | 7 |
| 216 | 48 | R64 | U5 | 5 | 237 | 56 | R45 | U6 | 6 |
| 215 | 49 | R39 | | 7 | 236 | 57 | R59 | | 4 |
| 228 | 50 | R61 | | 6 | 249 | 58 | R48 | | 5 |
| 229 | 51 | R43 | | 4 | 250 | 59 | R55 | | 7 |
| 211 | 52 | R38 | | 1 | 232 | 60 | R60 | | 0 |
| 212 | 53 | R65 | | 3 | 233 | 61 | R44 | | 2 |
| 224 | 54 | R62 | | 2 | 245 | 62 | R47 | | 1 |
| 225 | 55 | R42 | | 0 | 246 | 63 | R56 | | 3 |

4 Electrical Characteristics

This chapter contains speed grade definition, AC timing parameter and ODT tables.

4.1 Absolute Maximum Ratings

Attention: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 7 - Absolute Maximum Ratings

| Symbol | Parameter | Rating | | Unit | Note |
|-------------------|-----------------------------------------------|--------|------|------|------|
| | | Min. | Max. | | |
| V_{DD} | Voltage on V_{DD} pin relative to V_{SS} | -0.4 | +1.5 | V | |
| V_{DDQ} | Voltage on V_{DDQ} pin relative to V_{SS} | -0.4 | +1.5 | V | |
| V_{PP} | Voltage on V_{PP} pin relative to V_{SS} | -0.4 | 3.0 | V | |
| V_{IN}, V_{OUT} | Voltage on any pin relative to V_{SS} | -0.4 | +1.5 | V | |
| T_{STG} | Storage Temperature | - 50 | +100 | °C | |

Attention: Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to integrated circuit.

Table 8 - DRAM Component Operating Temperature Range

| Symbol | Parameter | Rating | | Unit | Note |
|------------|-----------------------|--------|------|------|----------|
| | | Min. | Max. | | |
| T_{CASE} | Operating Temperature | 0 | 95 | °C | 1)2)3)4) |

- 1) Operating Temperature is the case surface temperature on the center / top side of the DRAM.
- 2) The operating temperature ranges are the temperatures where all DRAM specification will be supported. During operation, the DRAM case temperature must be maintained between 0 - 95 °C under all other specification parameters.
- 3) Above 85 °C the Auto-Refresh command interval has to be reduced to $t_{REFI} = 3.9 \mu s$
- 4) When operating this product in the 85 °C to 95 °C T_{CASE} temperature range, the High Temperature Self Refresh has to be enabled by setting EMR(2) bit A7 to “1”.

4.2 Operating Conditions

Table 9 - Supply Voltage Levels and AC / DC Operating Conditions

| Parameter | Symbol | Values | | | Unit | Note |
|-------------------------|-------------------|----------------------|----------------------|----------------------|------|----------|
| | | Min. | Typ. | Max. | | |
| Device Supply Voltage | V_{DD} | 1.14 | 1.2 | 1.26 | V | 1),2),3) |
| Output Supply Voltage | V_{DDQ} | 1.14 | 1.2 | 1.26 | V | 1),2),3) |
| Peak-to-Peak Voltage | V_{PP} | 2.375 | 2.5 | 2.75 | V | 3) |
| Input Reference Voltage | V_{REF} | $0.49 \times V_{DD}$ | $0.5 \times V_{DDQ}$ | $0.51 \times V_{DD}$ | V | |
| DC Input Logic High | $V_{IH,CA}(DC65)$ | $V_{REFCA} + 0.065$ | — | V_{DD} | V | |
| DC Input Logic Low | $V_{IL,CA}(DC65)$ | Vss | — | $V_{REFCA} - 0.065$ | V | |
| AC Input Logic High | $V_{IH,CA}(AC90)$ | $V_{REF} + 0.09$ | — | | V | |
| AC Input Logic Low | $V_{IL,CA}(AC90)$ | | — | $V_{REF} - 0.09$ | V | |

Notes:

- 1) Under all conditions VDDQ must be less than or equal to VDD.
- 2) VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- 3) DC bandwidth is limited to 20MHz.

4.3 Module and Component Speed Grades

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

Table 10 - Module and Component Speed Grades

| Module Speed Grade | Component Speed Grade |
|---------------------------|------------------------------|
| -32AA | 3200-22-22-22 |

4.4 I_{DD} / I_{PP} Specifications and Conditions

List of tables defining I_{DD} / I_{PP} Specifications and Conditions.

Table 11 - I_{DD} / I_{PP} Measurement Conditions

| Symbol | Description |
|----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDD0 IPPO | Operating One Bank Active-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: High between ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern |
| IDD1 | Operating One Bank Active-Read-Precharge Current (AL=0) CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: High between ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern |
| IDD2N | Precharge Standby Current (AL=0) CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern |
| IDD2NT | Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern |
| IDD2P | Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0 |
| IDD2Q | Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0 |
| IDD3N IPP3N | Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern |
| IDD3P | Active Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0 |

| Symbol | Description |
|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDD4R | Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ² ; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern |
| IDD4W | Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern |
| IDD5R | Distributed Refresh Current (1X REF) CKE: HIGH; External clock: on; tCK, CL, nREFI: see the previous table; BL: 8 ¹ , AL: 0; CS_n: HIGH between REF; Command, address, bank group address, bank address inputs: partially toggling according to the IDD5R Measurement-Loop Pattern table; Data I/O: VDDQ; DM_n: stable at 1; Bank activity: REF command every nREFI (see the IDD5R Measurement-Loop Pattern table); Output buffer and RTT: enabled in mode registers ² ; ODT signal: stable at 0; Pattern details: see the IDD5R Measurement-Loop Pattern table |
| IDD6N | Self Refresh Current: Normal Temperature Range Tcase: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MIDLEVEL |
| IDD6E | Self-Refresh Current: Extended Temperature Range) TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL |
| IDD6R | Self-Refresh Current: Reduced Temperature Range TCase: 0 - 45°C; Low Power Array Self Refresh (LP ASR) : Reduced ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL |
| IDD6A | Auto Self-Refresh Current TCase: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL |
| IPP6x | Auto Self-Refresh Current TCase: -40 - 95°C; |

| Symbol | Description |
|--------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| IDD7 IPP7 | Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 8 ¹ ; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern |
| IDD8 | Maximum Power Down Current TBD |

Notes :

1. Burst Length: BL8 fixed by MRS: set MR0 [A1:0=00].
2. Output Buffer Enable - set MR1 [A12 = 0] : Qoff = Output buffer enabled - set MR1 [A2:1 = 00] : Output Driver Impedance Control = RZQ/7
 RTT_Nom enable - set MR1 [A10:8 = 011] : RTT_NOM = RZQ/6 RTT_WR enable - set MR2 [A10:9 = 01] : RTT_WR = RZQ/2 RTT_PARK
 disable - set MR5 [A8:6 = 000]
3. CAL enabled : set MR4 [A8:6 = 001] : 1600MT/s 010] : 1866MT/s, 2133MT/s 011] : 2400MT/s Gear Down mode enabled :set MR3 [A3 = 1] :
 1/4 Rate DLL disabled : set MR1 [A0 = 0] CA parity enabled :set MR5 [A2:0 = 001] : 1600MT/s,1866MT/s, 2133MT/s 010] : 2400MT/s Read
 DBI enabled : set MR5 [A12 = 1] Write DBI enabled : set :MR5 [A11 = 1]
4. Low Power Array Self Refresh (LP ASR) : set MR2 [A7:6 = 00] : Normal 01] : Reduced Temperature range 10] : Extended Temperature
 range 11] : Auto Self Refresh

Table 12 - IDD Specification for SCC08GS03G2F1C-32AA

| Product Type | SCC08GS03G2F1C-32AA | Unit | |
|--------------|---------------------|------|------|
| Organization | 8GB | | Note |
| | 1 Rank (×8) | | |
| | ×64 | | |
| | -32AA | | |
| Symbol | Current | | |
| IDD0 | TBD | mA | 2) |
| IDD1 | TBD | mA | 2) |
| IDD2N | TBD | mA | 3) |
| IDD2NT | TBD | mA | 2) |
| IDD2P | TBD | mA | 3) |
| IDD2Q | TBD | mA | 3) |
| IDD3N | TBD | mA | 3) |
| IDD3P | TBD | mA | 3) |
| IDD4R | TBD | mA | 2) |
| IDD4W | TBD | mA | 2) |
| IDD5B | TBD | mA | 2) |
| IDD5F2 | TBD | mA | 2) |
| IDD5F4 | TBD | mA | 2) |
| IDD6N | TBD | mA | 3) |
| IDD6E | TBD | mA | 3) |
| IDD6R | TBD | mA | 3) |
| IDD6A | TBD | mA | 3) |
| IDD7 | TBD | mA | 2) |
| IDD8 | TBD | mA | 3) |

- 1) Calculated values from Device data.
- 2) One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
- 3) All ranks in this IDD/IPP condition

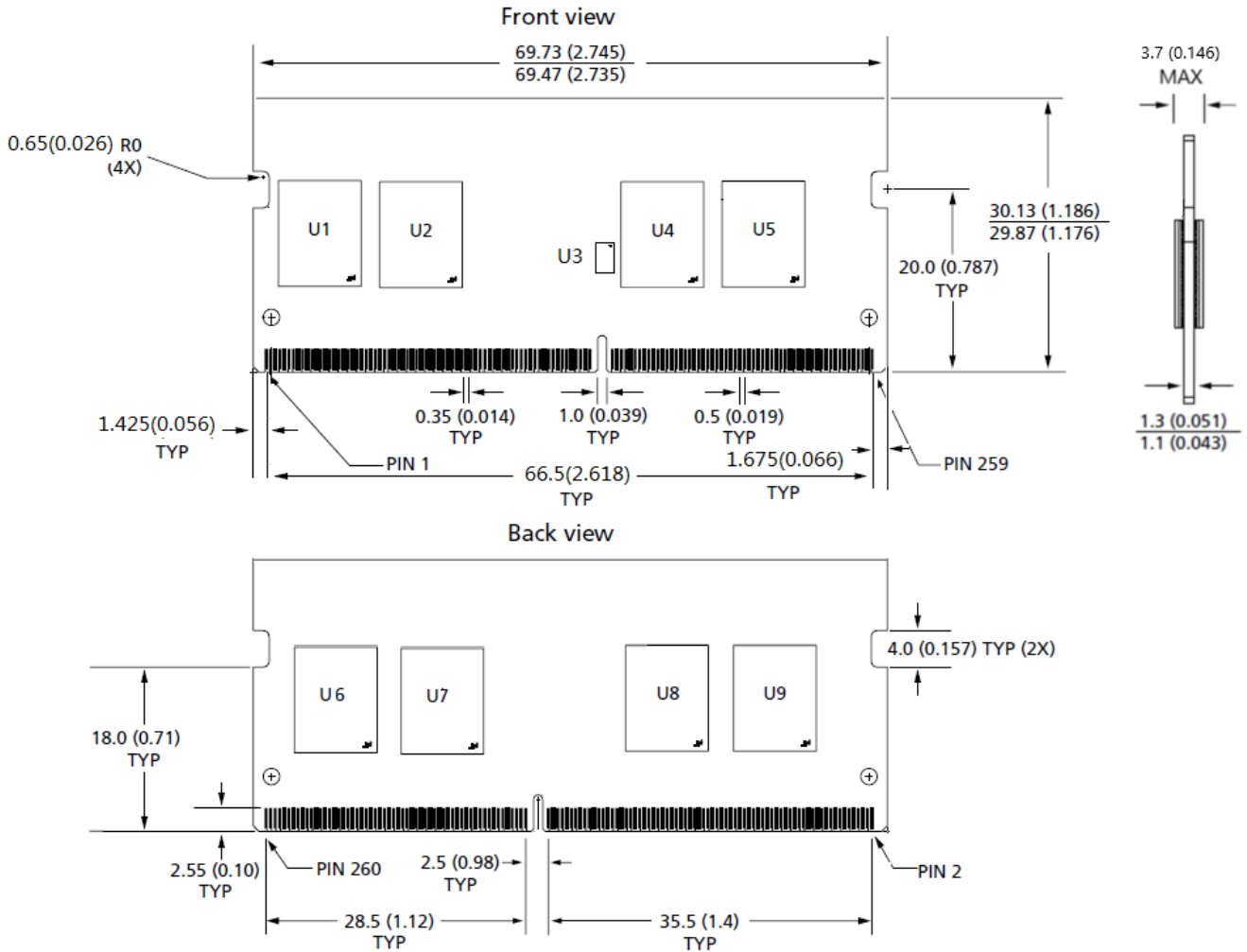
Table 13 - IPP Specification for SCC08GS03G2F1C-32AA

| Product Type | SCC08GS03G2F1C-32AA | Unit | |
|--------------|---------------------|------|------|
| Organization | 8GB | | Note |
| | 1 Rank (×8) | | |
| | ×64 | | |
| | -32AA | | |
| Symbol | Current | | |
| IPP0 | TBD | mA | 2) |
| IPP1 | TBD | mA | 2) |
| IPP2N | TBD | mA | 3) |
| IPP2P | TBD | mA | 3) |
| IPP3N | TBD | mA | 3) |
| IPP3P | TBD | mA | 3) |
| IPP4R | TBD | mA | 2) |
| IPP4W | TBD | mA | 2) |
| IPP5B | TBD | mA | 2) |
| IPP6N | TBD | mA | 3) |
| IPP6E | TBD | mA | 3) |
| IPP6R | TBD | mA | 3) |
| IPP6A | TBD | mA | 3) |
| IPP7 | TBD | mA | 2) |
| IPP8 | TBD | mA | 3) |

- 1) Calculated values from Device data.
- 2) One module rank in the active IDD/IPP, the other rank in IDD2P/IPP3N.
- 3) All ranks in this IDD/IPP condition

5 Package Dimensions

Figure 2 - Package Dimensions_SCC08GS03G2F1C-32AA



- Notes: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
 2. The dimensional diagram is for reference only.

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Edition 2025-10
Published by
Xi'an UnilC Semiconductors Co., Ltd.

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