Jul.2025

SCB11N4G160BF
SCB11R4G160BF
SCB11N8G322BF
SCB11R8G322BF

4Gbit/8Gbit LPDDR4/4X SDRAM
EU RoHS Compliant Products

Data Sheet

Rev. E

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2023-10	A	First version release
2024-07	B	Update temperature range. Update Product List table. Update command truth table ACT2 command definition.
2025-04	C	Update LPDDR4 IDD specification Add LPDDR4X IDD specification
2025-06	D	Add new PN for I grade
2025-07	E	Add commercial grade in product list

We Listen to Your Comments
Any information within this document that you feel is wrong, unclear or missing at all? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to: info@unisemicon.com

Contents

1 Overview

The UniIC LPDDR4/LPDDR4X SDRAM is organized as 1 or 2 channels per device, and individual channel is 8-banks and 16-bits. This product uses a double-data-rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 16n prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. This product offers fully synchronous operations referenced to both rising and falling edges of the clock. The data paths are internally pipelined and 16n bits prefetched to achieve very high bandwidth.

1.1 Features

The 4Gbit/8Gbit LPDDR4/LPDDR4X SDRAM offers the following key features:

- Configuration:
  - x32 for 2-channels per device
  - x16 for 1-channel per device
  - 8 internal banks per each channel
- Low-voltage Core and I/O Power Supplies
  - V_{DD1} = 1.70-1.95V
  - V_{DD2} = 1.06-1.17V
  - V_{DDQ} = 1.06-1.17V(LPDDR4)
  - V_{DDQ} = 0.57-0.65V(LPDDR4X)
- LVSTL(Low Voltage Swing Terminated Logic) I/O Interface
- Internal VREF and VREF Training
- Dynamic ODT :
  - DQ ODT :VSSQ Termination
  - CA ODT :VSS Termination
- Selectable output drive strength (DS)
- Max. Clock Frequency : 2133MHz (4266Mbps for one channel)
- 16-bit Pre-fetch DDR data bus
- Single data rate (multiple cycles) command/address bus
- Bidirectional/differential data strobe per byte of data (DQS, $\overline{DQS}$)
- DMI pin support for write data masking and DBI functionality
- Programmable READ and WRITE latencies (RL/WL)
- Programmable and on-the-fly burst lengths (BL =16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- ZQ Calibration
- Operation Temperature:
  - Commercial (T_C =0°C to 95°C)
  - Industrial (T_C = -40°C to 95°C)
  - Automotive A3 (T_C = -40°C to 95°C)
  - Automotive A2 (T_C = -40°C to 105°C)
- On-chip temperature sensor to control self-refresh rate
- On-chip temperature sensor whose status can be read from MR4
- 200-ball x16/x32 Discrete Package (10x14.5 mm)
- RoHS/REACH-compliant, “green” packaging

Table 1 - Operation frequency

Speed Grade	tCK (ns)	Freq.(MHz)	Data Rate(Mbps)
-06	0.625	1600	3200
-03	0.535	1866	3733
-04	0.468	2133	4266

*Other clock frequencies/data rates supported; please refer to AC timing tables

1.2 Product List

Table 2 shows all possible products within the 4Gbit/8Gbit LPDDR4/LPDDR4X SDRAM component generation. Availability depends on application needs. For UniIC part number nomenclatures see **Chapter** 5.

Table 2 - Ordering Information of LPDDR4

Product Type[1)]	Org.	Speed	READ latency DBI disabled	Clock (MHz)	Package	Note[2)]
Commercial Temperature Range (0°C to 95°C)						
SCB11N4G160BF-03A	×16	LPDDR4-3733	32	1866	PG-TFBGA-200	
SCB11N8G322BF-03A	×32					
SCB11N4G160BF-04Z	x16	LPDDR4-4266	36	2133		
SCB11N8G322BF-04Z	x32					
Industrial Temperature Range (-40°C to 95°C)						
SCB11N4G160BF-03AI	×16	LPDDR4-3733	32	1866	PG-TFBGA-200	
SCB11N8G322BF-03AI	×32					
SCB11N4G160BF-04ZI	x16	LPDDR4-4266	36	2133		
SCB11N8G322BF-04ZI	x32					
Automotive Temperature Range A3 (-40°C to 95°C)						
SCB11N4G160BF-03AA3	×16	LPDDR4-3733	32	1866	PG-TFBGA-200	
SCB11N8G322BF-03AA3	×32					
SCB11N4G160BF-04ZA3	×16	LPDDR4-4266	36	2133		
SCB11N8G322BF-04ZA3	×32					
Automotive Temperature Range A2 (-40°C to 105°C)						
SCB11N4G160BF-03AA2	×16	LPDDR4-3733	32	1866	PG-TFBGA-200	
SCB11N8G322BF-03AA2	×32					
SCB11N4G160BF-04ZA2	×16	LPDDR4-4266	36	2133		
SCB11N8G322BF-04ZA2	×32					

Table 3 - Ordering Information of LPDDR4X

Product Type[1)]	Org.	Speed	READ latency DBI disabled	Clock (MHz)	Package	Note[2)]
Commercial Temperature Range (0°C to 95°C)						
SCB11R4G160BF-03A	×16	LPDDR4X-3733	32	1866	PG-TFBGA-200	
SCB11R8G322BF-03A	×32					
SCB11R4G160BF-04Z	×16	LPDDR4X-4266	36	2133		
SCB11R8G322BF-04Z	×32					
Industrial Temperature Range (-40°C to 95°C)						
SCB11R4G160BF-03AI	×16	LPDDR4X-3733	32	1866	PG-TFBGA-200	
SCB11R8G322BF-03AI	×32					
SCB11R4G160BF-04ZI	×16	LPDDR4X-4266	36	2133		
SCB11R8G322BF-04ZI	×32					
Automotive Temperature Range A3 (-40°C to 95°C)						
SCB11R4G160BF-03AA3	×16	LPDDR4X-3733	32	1866	PG-TFBGA-200	
SCB11R8G322BF-03AA3	×32					
SCB11R4G160BF-04ZA3	×16	LPDDR4X-4266	36	2133		
SCB11R8G322BF-04ZA3	×32					
Automotive Temperature Range A2 (-40°C to 105°C)						
SCB11R4G160BF-03AA2	×16	LPDDR4X-3733	32	1866	PG-TFBGA-200	
SCB11R8G322BF-03AA2	×32					
SCB11R4G160BF-04ZA2	×16	LPDDR4X-4266	36	2133		
SCB11R8G322BF-04ZA2	×32					

1) For detailed information regarding product type of UniIC please see Chapter 5 “Product Type Nomenclature” of this data sheet.
2) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers. For more information please visit http://www.unisemicon.com/

Note：SCB11NxGxxxBF-xxxA2 and SCB11RxGxxxBF-xxxA2 meets AEC-Q100 reliability requirements. Detail qualification information refer to qualification report

1.3 Addressing

Table 4 - 4Gbit/8Gbit Addressing

Memory Density		4Gb	8Gb
Organization		x16	x32
Number of Channels		1	2
Density per channel		4Gb	4Gb
Configuration		32Mb x 16DQ x 8 banks x 1 channel	32Mb x 16DQ x 8 banks x 2 channels
Number of Banks (per Channel)		8	8
Array Pre-Fetch (Bits, per channel)		256	256
Number of Rows (per channel)		32,768	32,768
Number of Columns (fetch boundaries)		64	64
Page Size (Bytes)		2,048	2048
Bank Address		BA0-BA2	BA0-BA2
X16	Row Addresses	R0-R14	R0-R14
	Column Addresses	C0-C9	C0-C9
Burst Starting Address Boundary		64-bit	64-bit

Notes：

1. The lower two column addresses (C0 - C1) are assumed to be “zero” and are not transmitted on the CA bus.
2. Row and Column address values on the CA bus that are not used for a particular density be at valid logic levels.
3. For non - binary memory densities, only half of the row address space is valid. When the MSB address bit is “HIGH”, then the MSB - 1 address bit must be “LOW”.
4. The row address input which violates restriction described in note 3 may result in undefined or vendor specific behavior. Consult memory vendor for more information.

1.4 Package Block Diagram

Figure 1 – Dual Channel Package Block Diagram

Part number: SCB11N8G322BF / SCB11R8G322BF

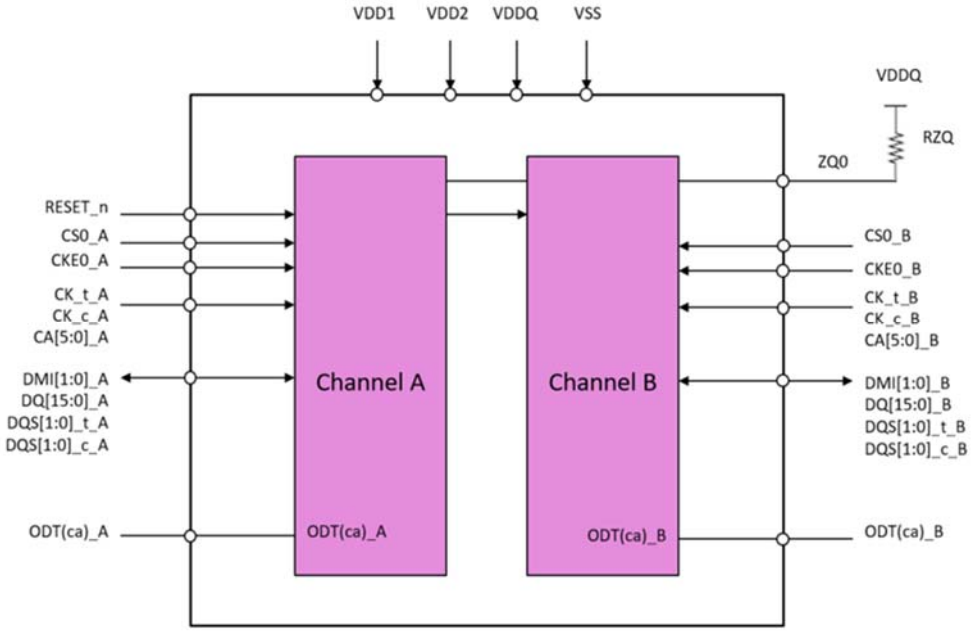
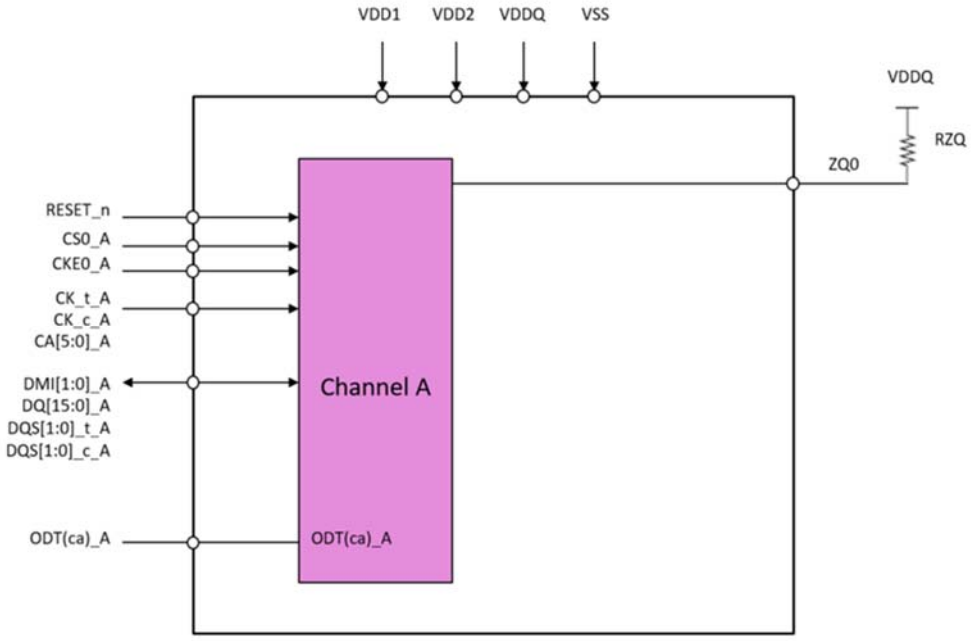


Figure 2 – Single Channel Package Block Diagram

Part number: SCB11N4G160BF / SCB11R4G160BF



1.5 Package Ballout

Figure 3 - 200-ball x32 Discrete Package, 0.80mm x 0.65mm using MO-311

0.80mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ0			NC	VDD2	VSS	NC	NC
B	NC	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	NC
C	VSS	DQ1 _A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1 _A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_T _A	VSS	VDDQ			VDDQ	VSS	DQS1_T _A	VSS	VDDQ
E	VSS	DQ2 _A	DQS0_C _A	DQ5_A	VSS			VSS	DQ13_A	DQS1_C _A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11 _A	VDD1
G	VSS	ODT_CA _A	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_A	NC	CS0_A	VDD2			VDD2	CA2 _A	CA3_A	CA4_A	VDD2
J	VSS	CA1_A	VSS	CKE0_A	NC			CK_t_A	CK_ c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
P	VSS	CA1_B	VSS	CKE0_B	NC			CK_t_B	CK_c_B	VSS	CA5_B	VSS
R	VDD2	CA0_B	NC	CS0_B	VDD2			VDD2	CA2_B	CA3_B	CA4_B	VDD2
T	VSS	ODT_CA _B	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_ n	VSS
U	VDD1	DQ3_B	VDDQ	DQ4_B	VDD2			VDD2	DQ12_B	VDDQ	DQ11_B	VDD1
V	VSS	DQ2_B	DQS0_C _B	DQ5_B	VSS			VSS	DQ13_B	DQS1_C _B	DQ10_B	VSS
W	VDDQ	VSS	DQS0_T _B	VSS	VDDQ			VDDQ	VSS	DQS1_T _B	VSS	VDDQ
Y	VSS	DQ1_B	DMI0_B	DQ6_B	VSS			VSS	DQ14_B	DMI1_B	DQ9_B	VSS
AA	NC	DQ0_B	VDDQ	DQ7_B	VDDQ			VDDQ	DQ15_B	VDDQ	DQ8_B	NC
AB	NC	NC	VSS	VDD2	VSS			VSS	VDD2	VSS	NC	NC

Notes:
1. 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.
2. Top View, A1 in top left corner.
3. ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package.
4. Die pad VSS and VSSQ signals are combined to VSS package balls.
5. The ODT_CA_[x] pins are ignored by LPDDR4X devices.

Figure 4 - 200-ball x16 Discrete Package, 0.80mm x 0.65mm using MO-311

0.80mm Pitch

	1	2	3	4	5	6	7	8	9	10	11	12
A	NC	NC	VSS	VDD2	ZQ0			NC	VDD2	VSS	NC	NC
B	NC	DQ0_A	VDDQ	DQ7_A	VDDQ			VDDQ	DQ15_A	VDDQ	DQ8_A	NC
C	VSS	DQ1 _A	DMI0_A	DQ6_A	VSS			VSS	DQ14_A	DMI1 _A	DQ9_A	VSS
D	VDDQ	VSS	DQS0_T _A	VSS	VDDQ			VDDQ	VSS	DQS1_T _A	VSS	VDDQ
E	VSS	DQ2 _A	DQS0_C _A	DQ5_A	VSS			VSS	DQ13_A	DQS1_C _A	DQ10_A	VSS
F	VDD1	DQ3_A	VDDQ	DQ4_A	VDD2			VDD2	DQ12_A	VDDQ	DQ11 _A	VDD1
G	VSS	ODT_CA _A	VSS	VDD1	VSS			VSS	VDD1	VSS	NC	VSS
H	VDD2	CA0_ A	NC	CS0_A	VDD2			VDD2	CA2 _A	CA3_A	CA4_A	VDD2
J	VSS	CA1 _ A	VSS	CKE0_A	NC			CK_t_A	CK_ c_A	VSS	CA5_A	VSS
K	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
L												
M												
N	VDD2	VSS	VDD2	VSS	NC			NC	VSS	VDD2	VSS	VDD2
P	VSS	NC	VSS	NC	NC			NC	NC	VSS	NC	VSS
R	VDD2	NC	NC	NC	VDD2			VDD2	NC	NC	NC	VDD2
T	VSS	NC	VSS	VDD1	VSS			VSS	VDD1	VSS	RESET_ n	VSS
U	VDD1	NC	VDDQ	NC	VDD2			VDD2	NC	VDDQ	NC	VDD1
V	VSS	NC	NC	NC	VSS			VSS	NC	NC	NC	VSS
W	VDDQ	VSS	NC	VSS	VDDQ			VDDQ	VSS	NC	VSS	VDDQ
Y	VSS	NC	NC	NC	VSS			VSS	NC	NC	NC	VSS
AA	NC	NC	VDDQ	NC	VDDQ			VDDQ	NC	VDDQ	NC	NC
AB	NC	NC	VSS	VDD2	VSS			VSS	VDD2	VSS	NC	NC

Notes:
1. 0.8mm pitch (X-axis), 0.65mm pitch (Y-axis), 22 rows.
2. Top View, A1 in top left corner.
3. ODT_CA_[x] balls are wired to ODT_CA_[x] pads of Rank 0 DRAM die. ODT_CA_[x] pads for other ranks (if present) are disabled in the package.
4. Die pad VSS and VSSQ signals are combined to VSS package balls.
5. The ODT_CA_A pin is ignored by LPDDR4X devices.

1.6 Pin Functional Description

Table 5 - Pin Functional Description

Symbol	Type	Function
CK_t_A, CK_c_A, CK_t_B, CK_c_B	Input	Clock: CK_t and CK_c are differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. AC timings for CA parameters are referenced to CK. Each channel (A & B) has its own clock pair.
CKE_A, CKE_B	Input	Clock Enable: CKE HIGH activates and CKE LOW deactivates the internal clock circuits, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is part of the command code. Each channel (A & B) has its own CKE signal.
CS_A, CS_B	Input	Chip Select: CS is part of the command code. Each channel (A & B) has its own CS signal.
CA[5:0]_A, CA[5:0]_B	Input	Command/Address Inputs: CA signals provide the Command and Address inputs according to the Command Truth Table. Each channel (A&B) has its own CA signals.
ODT_CA_A, ODT_CA_B	Input	LPDDR4 CA ODT Control: The ODT_CA pin is used in conjunction with the Mode Register to turn on/off the On-Die-Termination for CA pins. LPDDR4X CA ODT Control: The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to either VDD2 or VSS.
DQ[15:0]_A, DQ[15:0]_B	I/O	Data Input/Output: Bi-direction data bus.
DQS[1:0]_t_A, DQS[1:0]_c_A, DQS[1:0]_t_B, DQS[1:0]_c_B	I/O	Data Strobe: DQS_t and DQS_c are bi-directional differential output clock signals used to strobe data during a READ or WRITE. The Data Strobe is generated by the DRAM for a READ and is edge-aligned with Data. The Data Strobe is generated by the Memory Controller for a WRITE and must arrive prior to Data. Each byte of data has a Data Strobe signal pair. Each channel (A & B) has its own DQS strobes.
DMI[1:0]_A, DMI[1:0]_B	I/O	Data Mask Inversion: DMI is a bi-directional signal which is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. Data Inversion can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel (A & B) has its own DMI signals. This signal is also used along with the DQ signals to provide write data masking information to the DRAM. The DMI pin function - Data Inversion or Data mask - depends on Mode Register setting.
ZQ	Reference	Calibration Reference: Used to calibrate the output drive strength and the termination resistance. There is one ZQ pin per die. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ± 1% resistor.
VDDQ, VDD1, VDD2	Supply	Power Supplies: Isolated on the die for improved noise immunity.
VSS, VSSQ	GND	Ground Reference: Power supply ground reference.
RESET_n	Input	RESET: When asserted LOW, the RESET_n signal resets all channels of the die. There is one RESET_n pad per die.

Note : "_A" and "_B" indicate DRAM channel "_A" pads are present in all devices. "_B" pads are present in dual channel SDRAM devices only.

1.7 Command truth table

	SDR Command Pins	SDR CA Pins (6)							
SDRAM Command	CS	CA0	CA1	CA2	CA3	CA4	CA5	CK_t edge	Notes
Deselect (DES)	L	X						R1	1,2
Multi-Purpose Command (MPC)	H	L	L	L	L	L	OP6	R1	1,9
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Precharge (PRE) (Per Bank, All Bank)	H	L	L	L	L	H	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Refresh (REF) (Per Bank, All Bank)	H	L	L	L	H	L	AB	R1	1,2,3,4
	L	BA0	BA1	BA2	V	V	V	R2	
Self Refresh Entry (SRE)	H	L	L	L	H	H	V	R1	1,2
	L	V						R2	
Write -1 (WR-1)	H	L	L	H	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
Self Refresh Exit (SRX)	H	L	L	H	L	H	V	R1	1,2
	L	V						R2	
Mask Write -1 (MWR-1)	H	L	L	H	H	L	L	R1	1,2,3,5,6,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
RFU	H	L	L	H	H	H	V	R1	1,2
	L	V						R2	
Read -1 (RD-1)	H	L	H	L	L	L	BL	R1	1,2,3,6,7,9
	L	BA0	BA1	BA2	V	C9	AP	R2	
CAS-2 (Write-2, Mask Write -2, Read-2, MRR-2, MPC)	H	L	H	L	L	H	C8	R1	1,8,9
	L	C2	C3	C4	C5	C6	C7	R2	
RFU	H	L	H	L	H	L	V	R1	1,2
	L	V						R2	
RFU	H	L	H	L	H	H	V	R1	1,2
	L	V						R2	
Mode Register Write -1 (MRW-1)	H	L	H	H	L	L	OP7	R1	1,11
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
Mode Register Write-2 (MRW-2)	H	L	H	H	L	H	OP6	R1	1,11
	L	OP0	OP1	OP2	OP3	OP4	OP5	R2	
Mode Register Read-1 (MRR-1)	H	L	H	H	H	L	V	R1	1,2,12
	L	MA0	MA1	MA2	MA3	MA4	MA5	R2	
RFU	H	L	H	H	H	H	V	R1	1,2
	L	V						R2	
Activate -1 (ACT-1)	H	H	L	R12	R13	R14	R15	R1	1,2,3,10
	L	BA0	BA1	BA2	R16	R10	R11	R2	
Activate -2 (ACT-2)	H	H	H	R6	R7	R8	R9	R1	1,10
	L	R0	R1	R2	R3	R4	R5	R2	

Notes:

1. All LPDDR4 commands except for Deselect are 2 clock cycle long and defined by states of CS and CA[5:0] at the first rising edge of clock. Deselect command is 1 clock cycle long.
2. V" means "H" or "L" (a defined logic level). "X" means don't care in which case CA[5:0] can be floated.
3. Bank addresses BA[2:0] determine which bank is to be operated upon.
4. AB "HIGH" during Precharge or Refresh command indicates that command must be applied to all banks and bank address is a don't care.
5. Mask Write-1 command supports only BL 16. For Mark Write-1 command, CA5 must be driven LOW on first rising clock cycle (R1).
6. AP "HIGH" during Write-1, Mask Write-1 or Read-1 commands indicates that an Auto-Precharge will occur to the bank associated with the Write, Mask Write or Read command.

7. If Burst Length on-the-fly is enabled, BL "HIGH" during Write-1 or Read-1 command indicates that BurstLength should be set on-the-Fly to BL=32. BL "LOW" during Write-1 or Read-1 command indicates that Burst Length should be set on-the-fly to BL=16. If Burst Length on-the-fly is disabled, then BL must be driven to defined logic level "H" or "L".
8. For CAS-2 commands (Write-2 or Mask Write-2 or Read-2 or MRR-2 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration), C[1:0] are not transmitted on the CA[5:0] bus and are assumed to be zero. Note that for CAS-2 Write-2 or CAS-2 Mask Write-2 command, C[3:2] must be driven LOW.
9. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be immediately followed by CAS-2 command consecutively without any other command in between. Write-1 or Mask Write-1 or Read-1 or Mode Register Read-1 or MPC (Only Write FIFO, Read FIFO & Read DQ Calibration) command must be issued first before issuing CAS-2 command. MPC (Only Start & Stop DQS Oscillator, Start & Latch ZQ Calibration) commands do not require CAS-2 command; they require two additional DES or NOP commands consecutively before issuing any other commands.
10. Activate-1 command must be immediately followed by Activate-2 command consecutively without any other command in between. Activate-1 command must be issued first before issuing Activate-2 command. Once Activate-1 command is issued, Activate-2 command must be issued before issuing another Activate-1 command.
11. MRW-1 command must be immediately followed by MRW-2 command consecutively without any other command in between. MRW-1 command must be issued first before issuing MRW-2 command.
12. MRR-1 command must be immediately followed by CAS-2 command consecutively without any other command in between. MRR-1 command must be issued first before issuing CAS-2 command.

1.8 Power-up, Initialization and Power-off Procedure

For power-up and reset initialization, in order to prevent DRAM from functioning improperly, default values of the following MR settings are defined as **Table 6**.

Table 6 - MRS defaults settings

Item	MRS	Default Setting	Description
FSP-OP/WR	MR13 OP[7:6]	00_B	FSP-OP/WR[0] are enabled
WLS	MR2 OP[6]	0_B	Write Latency Set 0 is selected
WL	MR2 OP[5:3]	000_B	WL = 4
RL	MR2 OP[2:0]	000_B	RL = 6, nRTP=8
nWR	MR1 OP[6:4]	000_B	nWR = 6
DBI-WR/RD	MR3 OP[7:6]	00_B	Write & Read DBI are disabled
CA ODT	MR11 OP[6:4]	000_B	CA ODT is disabled
DQ ODT	MR11 OP[2:0]	000_B	DQ ODT is disabled
V_{REF}(CA) Setting	MR12 OP[6]	1_B	V_{REF}(CA) Range[1] enabled
V_{REF}(CA) Value	MR12 OP[5:0]	001101_B	Range1 : 27.2% of V_{DDQ} for LPDDR4
		011101_B	Range1 : 50.3% of V_{DDQ} for LPDDR4X
V_{REF}(DQ) Setting	MR14 OP[6]	1_B	V_{REF}(DQ) Range[1] enabled
V_{REF}(DQ) Value	MR14 OP[5:0]	001101_B	Range1 : 27.2% of V_{DDQ} for LPDDR4
		011101_B	Range1 : 50.3% of V_{DDQ} for LPDDR4X

1.8.1 Voltage Ramp and Device Initialization

The following sequence shall be used to power up the LPDDR4 device. Unless specified otherwise, these steps are mandatory. Note that the power-up sequence of all channels must proceed simultaneously.

1. While applying power (after Ta), RESET_n is recommended to be LOW (≤0.2 x V_{DD2}) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while RESET_nis held LOW. Power supply voltage ramp requirements are provided in **Table 7**. V_{DD1} must ramp at the same time or earlier than V_{DD2}. V_{DD2} must ramp at the same time or earlier than V_{DDQ}.

Table 7 - Voltage Ramp Conditions

After	Applicable Conditions
Ta is reached	V_{DD1} must be greater than V_{DD2}
	V_{DD2} must be greater than V_{DDQ} - 200 mV

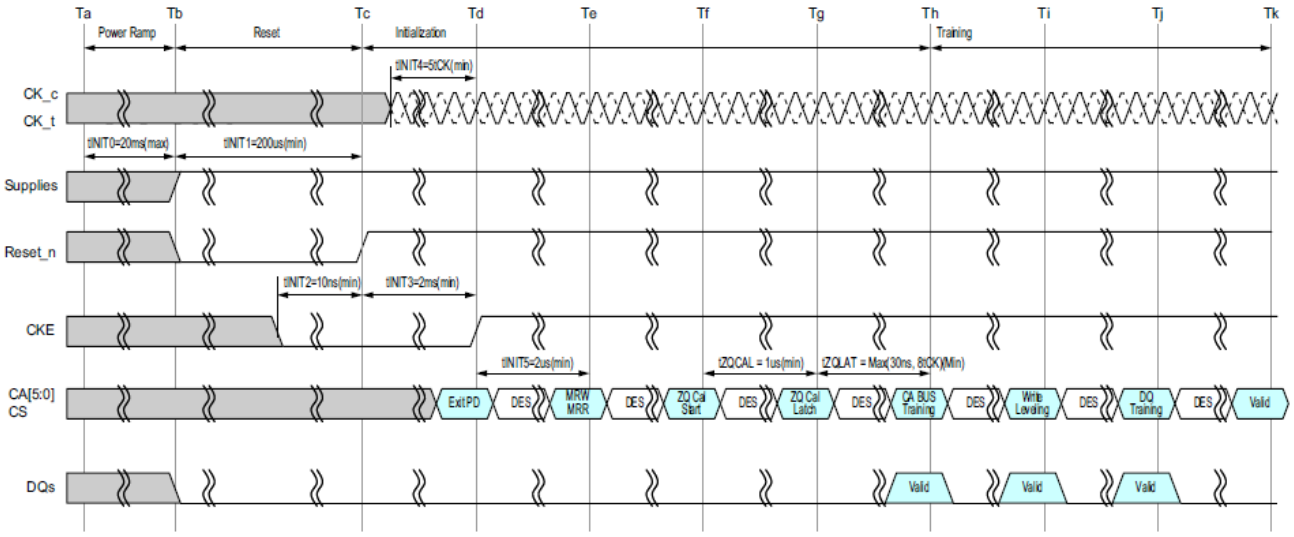
Notes:

1. Ta is the point when any power supply first reaches 300 mV.
2. Voltage ramp conditions in Table 8 apply between Ta and power-off (controlled or uncontrolled).
3. Tb is the point at which all supply and reference voltages are within their defined ranges.
4. Power ramp duration tINIT0 (Tb-Ta) must not exceed 20ms.
5. Thevoltage difference between any of V_{SS} and V_{SSQ} pins must not excess 100 mV.

2. Following the completion of the voltage ramp (Tb), RESET_n must be maintained LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch- up. CKE, CK_t, CK_c, CS_n and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

3. Beginning at Tb, RESET_n must remain LOW for at least tINIT1(Tc), after which RESET_n can be deasserted to HIGH(Tc). At least 10ns before RESET_n de-assertion, CKE is required to be set LOW. All other input signals are "Don't Care".

Figure 5 - Power Ramp and Initialization Sequence



Note : Training is optional and may be done at the system architects discretion. The training sequence after ZQ_CAL Latch(Th, Sequence7~9) in Figure 5 is simplified recommendation and actual training sequence may vary depending on systems.

4. After RESET_n is de-asserted(Tc), wait at least tINIT3 before activating CKE. Clock(CK_t,CK_c) is required to be started and stabilized for tINIT4 before CKE goes active(Td). CS is required to be maintained LOW when controller activates CKE.

5. After setting CKE high, wait minimum of tINIT5 to issue any MRR or MRW commands(Te). For both MRR and MRW commands, the clock frequency must be within the range defined for tCKb. Some AC parameters (for example, tDQSCK) could have relaxed timings (such as tDQSCKb) before the system is appropriately configured.

6. After completing all MRW commands to set the Pull-up, Pull-down and Rx termination values, the DRAM controller can issue ZQCAL Start command to the memory(Tf). This command is used to calibrate VOH level and output impedance over process, voltage and temperature. In systems where more than one LPDDR4 DRAM devices share one external ZQ resistor, the controller must not overlap the ZQ calibration sequence of each LPDDR4 device. ZQ calibration sequence is completed after tZQCAL (Tg) and the ZQCAL Latch command must be issued to update the DQ drivers and DQ+CA ODT to the calibrated values.

7. After tZQLAT is satisfied (Th) the command bus (internal V_{REF}(CA), CS, and CA) should be trained for high-speed operation by issuing an MRW command (Command Bus Training Mode). This command is used to calibrate the device's internal V_{REF} and align CS/CA with CK for high-speed operation. The LPDDR4 device will power-up with receivers configured for low-speed operations, and V_{REF}(CA) set to a default factory setting. Normal device operation at clock speeds higher than tCKb may not be possible until command bus training has been completed.

Note : The command bus training MRW command uses the CA bus as inputs for the calibration data stream, and outputs the results asynchronously on the DQ bus. See MRW for information on how to enter/exit the training mode.

8. After command bus training, DRAM controller must perform write leveling. Write leveling mode is enabled when MR2 OP[7] is high (Ti). See 4.31, Mode Register Write-WR Leveling Mode, for detailed description of write leveling entry and exit sequence. In write leveling mode, the DRAM controller adjusts write DQS_t/_c timing to the point where the LPDDR4 device recognizes the start of write DQ data burst with desired write latency.

9. After write leveling, the DQ Bus (internal V_{REF}(DQ), DQS, and DQ) should be trained for high-speed operation using the MPC training commands and by issuing MRW commands to adjust V_{REF}(DQ)(Tj). The LPDDR4 device will power-up with receivers configured for low-speed operations and V_{REF}(DQ) set to a default factory setting. Normal device operation at clock speeds higher than tCKb should not be attempted until DQ Bus training has been completed. The MPC Read Calibration command is used together with MPC FIFO Write/Read commands to train DQ bus without disturbing the memory array contents. See DQ Bus Training section for detailed DQ Bus Training sequence.

10. At Tk the LPDDR4 device is ready for normal operation, and is ready to accept any valid command. Any more registers that have not previously been set up for normal operation should be written at this time.

Table 8 - Initialization Timing Parameters

Parameter	Value		Unit	Comment
	Min	Max		
tINIT0	-	20	ms	Maximum voltage-ramp time
tINIT1	200	-	us	Minimum RESET_n LOW time after completion of voltage ramp
tINIT2	10	-	ns	Minimum CKE low time before RESET_n high
tINIT3	2	-	ms	Minimum CKE low time after RESET_n high
tINIT4	5	-	tCK	Minimum stable clock before first CKE high
tINIT5	2	-	us	Minimum idle time before first MRW/MRR command
tZQCAL	1	-	us	ZQ calibration time
tZQLAT	Max(30ns, 8tCK)	-	ns	ZQCAL latch quiet time.
tCKb	Note *1,2	Note *1,2	ns	Clock cycle time during boot

Notes:

1. Min tCKb guaranteed by DRAM test is 18 ns.
2. The system may boot at a higher frequency than dictated by min tCKb. The higher boot frequency is system dependent.

1.8.2 Reset Initialization with Stable Power

The following sequence is required for RESET at no power interruption initialization.

1. Assert RESET_n below 0.2 x V_{DD2} anytime when reset is needed. RESET_n needs to be maintained for minimum tPW_RESET. CKE must be pulled LOW at least 10 ns before de-asserting RESET_n.
2. Repeat steps 4 to 10 in 1.8.1 .

Table 9 - Reset Timing Parameter

Parameter	Value		Unit	Comment
	Min	Max		
tPW_RESET	100	-	ns	Minimum RESET_n low Time for Reset Initialization with stable power

1.8.3 Power-off Sequence

The following procedure is required to power off the device.

While powering off, CKE must be held LOW (0.2 X V_{DD2}) and all other inputs must be between VILmin and VIHmax. The device outputs remain at High-Z while CKE is held LOW. DQ, DMI, DQS_t and DQS_c voltage levels must be between V_{SSQ} and V_{DDQ} during voltage ramp to avoid latch-up. RESET_n, CK_t, CK_c, CS and CA input levels must be between V_{SS} and V_{DD2} during voltage ramp to avoid latch-up.

Tx is the point where any power supply drops below the minimum value specified.
Tz is the point where all power supplies are below 300mV. After Tz, the device is powered off.

Table 10 - Power Supply Conditions

After	Applicable Conditions
Tx and Tz	V_{DD1} must be greater than V_{DD2}
	VDD2 must be greater than VDDQ - 200 mV

The voltage difference between any of V_{SS}, V_{SSQ} pins must not exceed 100 mV.

1.8.4 Uncontrolled Power-off Sequence

When an uncontrolled power-off occurs, the following conditions must be met:

At Tx, when the power supply drops below the minimum values specified, all power supplies must be turned off and all power supply current capacity must be at zero, except any static charge remaining in the system.

After Tz (the point at which all power supplies first reach 300mV), the device must power off. During this period the relative

voltage between power supplies is uncontrolled. V_{DD1} and V_{DD2} must decrease with a slope lower than 0.5 V/µs between Tx and Tz.

An uncontrolled power-off sequence can occur a maximum of 400 times over the life of the device.

Table 11 - Timing Parameters Power Off

Symbol	Value		Unit	Comment
	Min	Max		
tPOFF	-	2	s	Maximum Power-off ramp item

1.9 Mode Register Definition

Table 12 shows the mode registers for LPDDR4/LPDDR4X SDRAM. Each register is denoted as "R" if it can be read but not written, "W" if it can be written but not read, and "R/W" if it can be read and written. A Mode Register Read command is used to read a mode register. A Mode Register Write command is used to write a mode register.

Table 12 - Mode Register Assignment in LPDDR4/LPDDR4X SDRAM

MR#	OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
0	CATR	RFU	RFU	RZQI		RFU	RFU	Refresh mode
1	RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	
2	WR Lev	WLS	WL			RL		
3	DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL
4	TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		
5	Manufacturer ID							
6	Revision ID-1							
7	Revision ID-2							
8	IO Width		Density			Type		
9	Vendor Specific Test Register							
10	RFU							ZQ-Reset
11	RFU	CA ODT			RFU	DQ ODT		
12	RFU	VR-CA	V_{REF}(CA)					
13	FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT
14	RFU	VR(dq)	V_{REF}(DQ)					
15	Lower-Byte Invert Register for DQ Calibration							
16	PASR Bank Mask							
17	PASR Segment Mask							
18	DQS Oscillator Count - LSB							
19	DQS Oscillator Count - MSB							
20	Upper-Byte Invert Register for DQ Calibration							
21	RFU							
22	RFU		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		
23	DQS interval timer run time setting							
24	TRR Mode	TRR Mode BAn			Unlimited MAC	MAC Value		
25	PPR Resource							
26	RFU							
27	RFU							
28	RFU							
29	RFU							
30	Reserved for testing - SDRAM will ignore							
31	RFU							
32	DQ Calibration Pattern “A” (default = 5AH)							
33	RFU							
34	RFU							
35	RFU							
36	RFU							
37	RFU							
38	RFU							
39	Reserved for testing - SDRAM will ignore							
40	DQ Calibration Pattern “B” (default = 3CH)							

MR0 Register Information (MA[5:0] = 00_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
CATR	RFU	RFU	RZQI		RFU	Latency Mode	Refresh mode

Function	Register Type	Operand	Data	Notes
Refresh mode	Read-only	OP[0]	0_B : Both legacy & modified refresh mode supported 1_B : Only modified refresh mode supported	
Latency Mode		OP[1]	0_B : Device supports normal latency 1_B : Device supports byte mode latency	6,7
RZQI (Built-in Self-Test for RZQ)		OP[4:3]	00_B: RZQ Self-Test Not Supported 01_B: ZQ pin may connect to V_{SSQ} or float 10_B: ZQ-pin may short to V_{DDQ} 11_B: ZQ-pin Self-Test Completed, no error condition detected (ZQ-pin may not connect to V_{SSQ} or float, nor short to V_{DDQ})	1,2,3,4
CATR (CA Terminating Rank)		OP[7]	0_B: CA for this rank is not terminated 1_B: Vendor specific	5

Notes:

1. RZQI MR value, if supported, will be valid after the following sequence:
   Completion of MPC ZQCAL Start command to either channel.
   Completion of MPC ZQCAL Latch command to either channel then tZQLAT is satisfied. RZQI value will be lost after Reset.
2. If the ZQ-pin is connected to VSSQ to set default calibration, OP[4:3] shall be set to 01B. If the ZQ-pin is not connected to VSSQ, either OP[4:3] = 01B or OP[4:3] = 10B might indicate a ZQ-pin assembly error. It is recommended that the assembly error is corrected.
3. In the case of possible assembly error, the LPDDR4-SDRAM device will default to factory trim settings for RON, and will ignore ZQ Calibration commands. In either case, the device may not function as intended.
4. If ZQ Self-Test returns OP[4:3] = 11B, the device has detected a resistor connected to the ZQ-pin. However, this result cannot be used to validate the ZQ resistor value or that the ZQ resistor tolerance meets the specified limits (i.e., 240Ω ± 1%).
5. CATR functionality is Vendor specific. CATR can either indicate the connection status of the ODTCA pad for the die or whether CA for the rank is terminated. Consult the vendor device datasheet for details.
6. See byte mode addendum spec for byte mode latency details.
7. Byte mode latency for 2Ch. x16 device is only allowed when it is stacked in a same package with byte mode device.

MR1 Register Information (MA[5:0] = 01_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RPST	nWR (for AP)			RD-PRE	WR-PRE	BL	

Function	Register Type	Operand	Data	Notes
BL (Burst Length)	Write-only	OP[1:0]	00_B: BL=16 Sequential (default) 01_B: BL=32 Sequential 10_B: BL=16 or 32 Sequential (on-the-fly) All Others: Reserved	1,5,6
WR-PRE (WR Pre-amble Length)		OP[2]	0_B: Reserved 1_B: WR Pre-amble = 2*tCK	5,6
RD-PRE (RD Pre-amble Type)		OP[3]	0_B: RD Pre-amble = Static (default) 1_B: RD Pre-amble = Toggle	3,5,6
nWR (Write-Recovery for Auto-Precharge commands)		OP[6:4]	000_B: nWR = 6 (default) 001_B: nWR = 10 010_B: nWR = 16 011_B: nWR = 20 100_B: nWR = 24 101_B: nWR = 30 110_B: nWR = 34 111_B: nWR = 40	2,5,6
RPST (RD Post-Amble Length)		OP[7]	0_B: RD Post-amble = 0.5*tCK (default) 1_B: RD Post-amble = 1.5*tCK	4,5,6

Notes:

1. Burst length on-the-fly can be set to either BL=16 or BL=32 by setting the “BL” bit in the command operands. See the Command Truth Table.
2. The programmed value of nWR is the number of clock cycles the LPDDR4-SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (auto-precharge) enabled.
3. For Read operations this bit must be set to select between a "toggling" pre-amble and a "Non-toggling" Pre-amble. See 4.5, Read Preamble and Postamble, for a drawing of each type of pre-amble.
4. OP[7] provides an optional READ post-amble with an additional rising and falling edge of DQS_t. The optional postamble cycle is provided for the benefit of certain memory controllers.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 13 - Burst Sequence for READ

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																																	
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																		
		V	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3																		
		V	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7																		
		V	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B																		
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F
		0	0	1	0	0	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13
		0	1	0	0	0	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17
		0	1	1	0	0	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B
		1	0	0	0	0	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
		1	0	1	0	0	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	4	5	6	7	8	9	A	B	C	D	E	F	0	1	2	3
		1	1	0	0	0	18	19	1A	1B	1C	1D	1E	1F	10	11	12	13	14	15	16	17	8	9	A	B	C	D	E	F	0	1	2	3	4	5	6	7
		1	1	1	0	0	1C	1D	1E	1F	10	11	12	13	14	15	16	17	18	19	1A	1B	C	D	E	F	0	1	2	3	4	5	6	7	8	9	A	B

Notes:
1. C0-C1 are assumed to be '0', and are not transmitted on the command bus.
2. The starting burst address is on 64-bit (4n) boundaries.

Table 14 - Burst Sequence for Write

Burst Length	Burst Type	C4	C3	C2	C1	C0	Burst Cycle Number and Burst Address Sequence																																	
							1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
16	SEQ	V	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F																		
32	SEQ	0	0	0	0	0	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F

Notes:
1. C0-C1 are assumed to be '0', and are not transmitted on the command bus.
2. The starting address is on 256-bit (16n) boundaries for Burst length 16.
3. The starting address is on 512-bit (32n) boundaries for Burst length 32.
4. C2-C3 shall be set to '0' for all Write operations.

MR2 Register Information (MA[5:0] = 02_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
WR Lev	WLS	WL			RL		

Function	Register Type	Operand	Data	Notes
RL (Read latency)	Write-only	OP[2:0]	RL & nRTP for DBI-RD Disabled (MR3 OP[6]=0_B) 000_B: RL=6, nRTP = 8 (Default) 001_B: RL=10, nRTP = 8 010_B: RL=14, nRTP = 8 011_B: RL=20, nRTP = 8 100_B: RL=24, nRTP = 10 101_B: RL=28, nRTP = 12 110_B: RL=32, nRTP = 14 111_B: RL=36, nRTP = 16 RL & nRTP for DBI-RD Enabled (MR3 OP[6]=1_B) 000_B: RL=6, nRTP = 8 001_B: RL=12, nRTP = 8 010_B: RL=16, nRTP = 8 011_B: RL=22, nRTP = 8 100_B: RL=28, nRTP = 10 101_B: RL=32, nRTP = 12 110_B: RL=36, nRTP = 14 111_B: RL=40, nRTP = 16	1,3,4
WL (Write latency)		OP[5:3]	WL Set "A" (MR2 OP[6]=0_B) 000_B: WL=4 (Default) 001_B: WL=6 010_B: WL=8 011_B: WL=10 100_B: WL=12 101_B: WL=14 110_B: WL=16 111_B: WL=18 WL Set "B" (MR2 OP[6]=1_B) 000_B: WL=4 001_B: WL=8 010_B: WL=12 011_B: WL=18 100_B: WL=22 101_B: WL=26 110_B: WL=30 111_B: WL=34	1,3,4
WLS (Write Latency Set)		OP[6]	0_B: WL Set "A" (default) 1_B: WL Set "B"	1,3,4
WR LEV (Write Leveling)		OP[7]	0_B: Disabled (default) 1_B: Enabled	2

Notes:
1. See Table 50 Read and Write Latencies for detail.
2. After a MRW to set the Write Leveling Enable bit (OP[7]=1B), the LPDDR4-SDRAM device remains in the MRW state until another MRW command clears the bit (OP[7]=0B). No other commands are allowed until the Write Leveling Enable bit is cleared.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
4. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR3 Register Information (MA[5:0] = 03_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DBI-WR	DBI-RD	PDDS			PPRP	WR PST	PU-CAL

Function	Register Type	Operand	Data	Notes
PU-Cal (LPDDR4) (Pull-up Calibration Point)	Write-only	OP[0]	0_B: V_{DDQ}/2.5 1_B: V_{DDQ}/3 (default)	1,4
PU-Cal (LPDDR4X) (Pull-up Calibration Point)		OP[0]	0_B: V_{DDQ}*0.6 1_B: V_{DDQ}*0.5 (default)	1,4
WR PST(WR Post-Amble Length)		OP[1]	0_B: WR Post-amble = 0.5*tCK (default) 1_B: WR Post-amble = 1.5*tCK(Vendor specific)	2,3,5
Post Package Repair Protection		OP[2]	0_B: PPR protection disabled (default) 1_B: PPR protection enabled	6
PDDS (Pull-Down Drive Strength)		OP[5:3]	000_B: RFU 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 (default) 111_B: Reserved	1,2,3
DBI-RD (DBI-Read Enable)		OP[6]	0_B: Disabled (default) 1_B: Enabled	2,3
DBI-WR (DBI-Write Enable)		OP[7]	0_B: Disabled (default) 1_B: Enabled	2,3

Notes:
1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. For dual channel devices, PU-CAL setting is required as the same value for both Ch.A and Ch.B before issuing ZQ Cal start command.
5. Refer to the supplier data sheet for vender specific function. 1.5*tCK apply > 1.6GHz clock.
6. If MR3 OP[2] is set to 1b then PPR protection mode is enabled. The PPR Protection bit is a sticky bit and can only be set to 0b by a power on reset.
   MR4 OP[4] controls entry to PPR Mode. If PPR protection is enabled then DRAM will not allow writing of 1 to MR4 OP[4].

MR4 Register Information (MA[5:0] = 04_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TUF	Thermal Offset		PPRE	SR Abort	Refresh Rate		

Function	Register Type	Operand	Data	Notes
Refresh Rate	Read	OP[2:0]	000_B: SDRAM Low temperature operating limit exceeded 001_B: 4x refresh 010_B: 2x refresh 011_B: 1x refresh (default) 100_B: 0.5x refresh 101_B: 0.25x refresh, no de-rating 110_B: 0.25x refresh, with de-rating 111_B: SDRAM High temperature operating limit exceeded	1,2,3,4, 7,8,9
SR Abort (Self Refresh Abort)	Write	OP[3]	0_B: Disable (default) 1_B: Enable	9,11
PPRE (Post-package repair entry/exit)	Write	OP[4]	0_B: Exit PPR mode (default) 1_B: Enter PPR mode	5,9
Thermal Offset (Vender Specific Function)	Write	OP[6:5]	00_B: No offset, 0~5°C gradient (default) 01_B: 5°C offset, 5~10°C gradient 10_B: 10°C offset, 10~15°C gradient 11_B: Reserved	10
TUF (Temperature Update Flag)	Read	OP[7]	0_B: No change in OP[2:0] since last MR4 read (default) 1_B: Change in OP[2:0] since last MR4 read	6,7,8

Notes:

1. The refresh rate for each MR4-OP[2:0] setting applies to tREFI, tREFIpb, and tREFW. OP[2:0]=011B corresponds to a device temperature of 85 °C. Other values require either a longer (2x, 4x) refresh interval at lower temperatures, or a shorter (0.5x, 0.25x) refresh interval at higher temperatures. If OP[2]=1B, the device temperature is greater than 85 °C.
2. At higher temperatures (>85 °C), AC timing derating may be required. If derating is required the LPDDR4-SDRAM will set OP[2:0]=110_B.
3. DRAM vendors may or may not report all of the possible settings over the operating temperature range of the device. Each vendor guarantees that their device will work at any temperature within the range using the refresh interval requested by their device.
4. The device may not operate properly when OP[2:0]=000_B or 111_B.
5. Post-package repair can be entered or exited by writing to OP[4].
6. When OP[7]=1, the refresh rate reported in OP[2:0] has changed since the last MR4 read. A mode register read from MR4 will reset OP[7] to '0'.
7. OP[7] = 0 at power-up. OP[2:0] bits are valid after initialization sequence(Te).
8. See the section on “temperature Sensor” for information on the recommended frequency of reading MR4.
9. OP[6:3] bits that can be written in this register. All other bits will be ignored by the DRAM during a MRW to this register.
10. Refer to the supplier data sheet for vender specific function.
11. Self Refresh abort feature is available for higher density devices starting with 12Gb device.

MR5 Register Information (MA[5:0] = 05_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Manufacturer ID							

Function	Register Type	Operand	Data	Function
Manufacturer ID	Read-Only	OP[7:0]	$0001\ 1010_B$: UniIC All Others: Reserved	Manufacturer ID

MR6 Register Information (MA[7:0] = 06_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-1							

Function	Register Type	Operand	Data	Notes
LPDDR4 Revision ID-1	Read-only	OP[7:0]	00000000_B: A-version 00000001_B: B-version	1

Note 1: MR6 is vendor specific.

MR7 Register Information (MA[7:0] = 07_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Revision ID-2							

Function	Register Type	Operand	Data	Notes
LPDDR4 Revision ID-2	Read-only	OP[7:0]	00000000_B: A-version 00000001_B: B-version	1

Note 1: MR7 is vendor specific.

MR8 Register Information (MA[5:0] = 08_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
IO Width		Density				Type	

Function	Register Type	Operand	Data	Notes
Type	Read-only	OP[1:0]	00_B: S16 SDRAM (16n pre-fetch) All Others: Reserved	
Density		OP[5:2]	0000_B: 4Gb dual channel die / 2Gb single channel die 0001_B: 6Gb dual channel die / 3Gb single channel die 0010_B: 8Gb dual channel die / 4Gb single channel die 0011_B: 12Gb dual channel die / 6Gb single channel die 0100_B: 16Gb dual channel die / 8Gb single channel die 0101_B: 24Gb dual channel die / 12Gb single channel die 0110_B: 32Gb dual channel die / 16Gb single channel die All Others: Reserved	
IO Width		OP[7:6]	00_B: x16 (per channel) All Others: Reserved	

MR9 Register Information (MA[7:0] = 09_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Vendor Specific Test Register							

Note : Only 00_H should be written to this register.

MR10 Register Information (MA[7:0] = $0A_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU							ZQ-Reset

Function	Register Type	Operand	Data	Notes
ZQ-Reset	Write-only	OP[0]	0_B: Normal Operation (Default) 1_B: ZQ Reset	1

Note 1: If the ZQ-pin is connected to V_{DDQ} through R_{ZQ}, either the ZQ calibration function or default calibration (via ZQ-Reset) is supported. If the ZQ-pin is connected to V_{SS}, the device operates with default calibration, and ZQ calibration commands are ignored. In both cases, the ZQ connection shall not change after power is applied to the device.

MR11 Register Information (MA[5:0] = $0B_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	CA ODT			RFU	DQ ODT		

Function	Register Type	Operand	Data	Notes
DQ ODT (DQ Bus Receiver On-Die-Termination)	Write-only	OP[2:0]	000_B: Disable (Default) 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 111_B: RFU	1,2,3
CA ODT (CA Bus Receiver On-Die-Termination)	Write-only	OP[6:4]	000_B: Disable (Default) 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 111_B: RFU	1,2,3

Notes:

1. All values are "typical". The actual value after calibration will be within the specified tolerance for a given voltage and temperature. Re-calibration may be required as voltage and temperature vary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR12 Register Information (MA[5:0] = $0C_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR-CA	V_{REF}(CA)					

Function	Register Type	Operand	Data	Notes
V_{REF}(CA) (V_{REF}(CA) Setting)	Read/ Write	OP[5:0]	000000_B: -- Thru -- 110010_B: See table below All Others: Reserved	1,2,3, 5,6
VR-CA (V_{REF}(CA) Range)		OP[6]	0_B: V_{REF}(CA) Range[0] enabled 1_B: V_{REF}(CA) Range[1] enabled (default)	1,2,4, 5,6

Notes:

1. This register controls the V_{REF}(CA) levels. Refer to **Table 15** - VREF Settings for Range[0] and Range[1] for actual voltage of V_{REF}(CA).
2. A read to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to '0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal V_{REF}(CA) level for FSP[0] when MR13 OP[6]=0_B, or sets FSP[1] when MR13 OP[6]=1_B. The time required for V_{REF}(CA) to reach the set level depends on the step size from the current level to the new level. See the section on V_{REF}(CA) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal V_{REF}(CA) ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}(CA) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

Table 15 - V_{REF} Settings for Range[0] and Range[1] for LPDDR4

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
V_{REF} Settings for MR12 and MR14	OP[5:0]	000000_B: 10.0%	011010_B: 20.4%	000000_B: 22.0%	011010_B: 32.4%	1,2,3
		000001_B: 10.4%	011011_B: 20.8%	000001_B: 22.4%	011011_B: 32.8%	
		000010_B: 10.8%	011100_B: 21.2%	000010_B: 22.8%	011100_B: 33.2%	
		000011_B: 11.2%	011101_B: 21.6%	000011_B: 23.2%	011101_B: 33.6%	
		000100_B: 11.6%	011110_B: 22.0%	000100_B: 23.6%	011110_B: 34.0%	
		000101_B: 12.0%	011111_B: 22.4%	000101_B: 24.0%	011111_B: 34.4%	
		000110_B: 12.4%	100000_B: 22.8%	000110_B: 24.4%	100000_B: 34.8%	
		000111_B: 12.8%	100001_B: 23.2%	000111_B: 24.8%	100001_B: 35.2%	
		001000_B: 13.2%	100010_B: 23.6%	001000_B: 25.2%	100010_B: 35.6%	
		001001_B: 13.6%	100011_B: 24.0%	001001_B: 25.6%	100011_B: 36.0%	
		001010_B: 14.0%	100100_B: 24.4%	001010_B: 26.0%	100100_B: 36.4%	
		001011_B: 14.4%	100101_B: 24.8%	001011_B: 26.4%	100101_B: 36.8%	
		001100_B: 14.8%	100110_B: 25.2%	001100_B: 26.8%	100110_B: 37.2%	
		001101_B: 15.2%	100111_B: 25.6%	001101_B: 27.2% (Default)	100111_B: 37.6%	
		001110_B: 15.6%	101000_B: 26.0%	001110_B: 27.6%	101000_B: 38.0%	
		001111_B: 16.0%	101001_B: 26.4%	001111_B: 28.0%	101001_B: 38.4%	

Function	Operand	Range[0] Values (% of VDDQ)		Range[1] Values (% of VDDQ)		Notes
		010000_B: 16.4%	101010_B: 26.8%	010000_B: 28.4%	101010_B: 38.8%	
		010001_B: 16.8%	101011_B: 27.2%	010001_B: 28.8%	101011_B: 39.2%	
		010010_B: 17.2%	101100_B: 27.6%	010010_B: 29.2%	101100_B: 39.6%	
		010011_B: 17.6%	101101_B: 28.0%	010011_B: 29.6%	101101_B: 40.0%	
		010100_B: 18.0%	101110_B: 28.4%	010100_B: 30.0%	101110_B: 40.4%	
		010101_B: 18.4%	101111_B: 28.8%	010101_B: 30.4%	101111_B: 40.8%	
		010110_B: 18.8%	110000_B: 29.2%	010110_B: 30.8%	110000_B: 41.2%	
		010111_B: 19.2%	110001_B: 29.6%	010111_B: 31.2%	110001_B: 41.6%	
		011000_B: 19.6%	110010_B: 30.0%	011000_B: 31.6%	110010_B: 42.0%	
		011001_B: 20.0%	All Others: Reserved	011001_B: 32.0%	All Others: Reserved	

Notes:
1. These values may be used for MR12 OP[5:0] and MR14 OP[5:0] to set the V_{REF}(CA) or V_{REF} (DQ) levels in the device.
2. The range may be selected in the MR12 or MR14 register by setting OP[6] appropriately.
3. The MR12 or MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation, or between different high-frequency setting which may use different terminations values.

Table 16 – V_{REF} Settings for Range[0] and Range[1] for LPDDR4X

Function	Operand	Range[0] Values (% of V_{DDQ})		Range[1] Values (% of V_{DDQ})		Notes
V_{REF} Settings for MR12 and MR14	OP[5:0]	000000_B: 15.0%	011010_B: 30.5%	000000_B: 32.9%	011010_B b: 48.5%	1,2,3
		000001_B: 15.6%	011011_B: 31.1%	000001_B: 33.5%	011011_B: 49.1%	
		000010_B: 16.2%	011100_B: 31.7%	000010_B: 34.1%	011100_B: 49.7%	
		000011_B: 16.8%	011101_B: 32.3%	000011_B: 34.7%	011101_B: 50.3% (Default)	
		000100_B: 17.4%	011110_B: 32.9%	000100_B: 35.3%	011110_B: 50.9%	
		000101_B: 18.0%	011111_B: 33.5%	000101_B: 35.9%	011111_B: 51.5%	
		000110_B: 18.6%	100000_B: 34.1%	000110_B: 36.5%	100000_B: 52.1%	
		000111_B: 19.2%	100001_B: 34.7%	000111_B: 37.1%	100001_B: 52.7%	
		001000_B: 19.8%	100010_B: 35.3%	001000_B: 37.7%	100010_B: 53.3%	
		001001_B: 20.4%	100011_B: 35.9%	001001_B: 38.3%	100011_B: 53.9%	
		001010_B: 21.0%	100100_B: 36.5%	001010_B: 38.9%	100100_B: 54.5%	
		001011_B: 21.6%	100101_B: 37.1%	001011_B: 39.5%	100101_B: 55.1%	
		001100_B: 22.2%	100110_B: 37.7%	001100_B: 40.1%	100110_B: 55.7%	
		001101_B: 22.8%	100111_B: 38.3%	001101_B: 40.7%	100111_B: 56.3%	
		001110_B: 23.4%	101000_B: 38.9%	001110_B: 41.3%	101000_B: 56.9%	
		001111_B: 24.0%	101001_B: 39.5%	001111_B: 41.9%	101001_B: 57.5%	
		010000_B: 24.6%	101010_B: 40.1%	010000_B: 42.5%	101010_B: 58.1%	
		010001_B: 25.1%	101011_B: 40.7%	010001_B: 43.1%	101011_B: 58.7%	
		010010_B: 25.7%	101100_B: 41.3%	010010_B: 43.7%	101100_B: 59.3%	
		010011_B: 26.3%	101101_B: 41.9%	010011_B: 44.3%	101101_B: 59.9%	
		010100_B: 26.9%	101110_B: 42.5%	010100_B: 44.9%	101110_B: 60.5%	
		010101_B: 27.5%	101111_B: 43.1%	010101_B: 45.5%	101111_B: 61.1%	
		010110_B: 28.1%	110000_B: 43.7%	010110_B: 46.1%	110000_B: 61.7%	
		010111_B: 28.7%	110001_B: 44.3%	010111_B: 46.7%	110001_B: 62.3%	
		011000_B: 29.3%	110010_B: 44.9%	011000_B: 47.3%	110010_B: 62.9%	
		011001_B: 29.9%	All Others: Reserved	011001_B: 47.9%	All others: Reserved	

Notes:
1. These values may be used for MR12 OP[5:0] and MR14 OP[5:0] to set the V_{REF}(CA) or V_{REF} (DQ) levels in the device.

2. The range may be selected in the MR12 or MR14 register by setting OP[6] appropriately.
3. The MR12 or MR14 registers represents either FSP[0] or FSP[1]. Two frequency-set-points each for CA and DQ are provided to allow for faster switching between terminated and unterminated operation, or between different high-frequency setting which may use different terminations values.

MR13 Register Information (MA[5:0] = $0D_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
FSP-OP	FSP-WR	DMD	RRO	VRCG	VRO	RPT	CBT

Function	Register Type	Operand	Data	Notes
CBT (Command Bus Training)	Write-only	OP[0]	0_B: Normal Operation (default) 1_B: Command Bus Training Mode Enabled	1
RPT (Read Preamble Training Mode)		OP[1]	0_B : Disable (default) 1_B : Enable	
VRO (V_{REF} Output)		OP[2]	0_B: Normal operation (default) 1_B: Output the V_{REF}(CA) and V_{REF}(DQ) values on DQ bits	2
VRCG (V_{REF} Current Generator)		OP[3]	0_B: Normal Operation (default) 1_B: V_{REF} Fast Response (high current) mode	3
RRO Refresh rate option		OP[4]	0_B: Disable codes 001 and 010 in MR4 OP[2:0] 1_B: Enable all codes in MR4 OP[2:0]	4, 5
DMD (Data Mask Disable)		OP[5]	0_B: Data Mask Operation Enabled (default) 1_B: Data Mask Operation Disabled	6
FSP-WR (Frequency Set Point Write/Read)		OP[6]	0_B: Frequency-Set-Point[0] (default) 1_B: Frequency-Set-Point [1]	7
FSP-OP (Frequency Set Point Operation Mode)		OP[7]	0_B: Frequency-Set-Point[0] (default) 1_B: Frequency-Set-Point [1]	8

Notes:

1. A write to set OP[0]=1 causes the LPDDR4-SDRAM to enter the Command Bus Training mode. When OP[0]=1 and CKE goes LOW, commands are ignored and the contents of CA[5:0] are mapped to the DQ bus. CKE must be brought HIGH before doing a MRW to clear this bit (OP[0]=0) and return to normal operation. See the Command Bus Training section for more information.
2. When set, the LPDDR4-SDRAM will output the V_{REF}(CA) and V_{REF}(DQ) voltages on DQ pins. Only the “active” frequency-set-point, as defined by MR13 OP[7], will be output on the DQ pins. This function allows an external test system to measure the internal V_{REF} levels. The DQ pins used for V_{REF} output are vendor specific.
3. When OP[3]=1, the V_{REF} circuit uses a high-current mode to improve V_{REF} settling time.
4. MR13 OP4 RRO bit is valid only when MR0 OP0 = 1. For LPDDR4 devices with MR0 OP0 = 0, MR4 OP[2:0] bits are not dependent on MR13 OP4.
5. When OP[4] = 0, only 001b and 010b in MR4 OP[2:0] are disabled. LPDDR4 devices must report 011b instead of 001b or 010b in this case. Controller should follow the refresh mode reported by MR4 OP[2:0], regardless of RRO setting. TCSR function does not depend on RRO setting.
6. When enabled (OP[5]=0B) data masking is enabled for the device. When disabled (OP[5]=1B), masked write command is illegal.
7. FSP-WR determines which frequency-set-point registers are accessed with MRW commands for the following functions such as V_{REF}(CA) Setting, V_{REF}(CA) Range, V_{REF}(DQ) Setting, V_{REF}(DQ) Range.
8. FSP-OP determines which frequency-set-point register values are currently used to specify device operation for the following functions such as V_{REF}(CA) Setting, V_{REF}(CA) Range, V_{REF}(DQ) Setting, V_{REF}(DQ) Range.

MR14 Register Information (MA[5:0] = $0E_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU	VR(DQ)	V_{REF}(DQ)					

Function	Register Type	Operand	Data	Notes
V_{REF}(DQ) (V_{REF}(DQ) Setting)	Read/ Write	OP[5:0]	000000_B: -- Thru -- 110010_B: See table below All Others: Reserved	1,2,3, 5,6
VR(dq) (V_{REF}(DQ) Range)		OP[6]	0_B: V_{REF}(DQ) Range[0] enabled 1_B: V_{REF}(DQ) Range[1] enabled (default)	1,2,4, 5,6

Notes:
1. This register controls the V_{REF}(DQ) levels for Frequency-Set-Point[1:0]. Values from either VR(DQ)[0] or VR(dq)[1] may be selected by setting OP[6] appropriately.
2. A read (MRR) to this register places the contents of OP[7:0] on DQ[7:0]. Any RFU bits and unused DQ's shall be set to'0'. See the section on MRR Operation.
3. A write to OP[5:0] sets the internal V_{REF}(DQ) level for FSP[0] when MR13 OP[6]=0B, or sets FSP[1] when MR13 OP[6]=1B. The time required for V_{REF}(DQ) to reach the set level depends on the step size from the cur- rent level to the new level. See the section on V_{REF}(DQ) training for more information.
4. A write to OP[6] switches the LPDDR4-SDRAM between two internal V_{REF}(DQ) ranges. The range (Range[0] or Range[1]) must be selected when setting the V_{REF}(DQ) register. The value, once set, will be retained until overwritten, or until the next power-on or RESET event.
5. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
6. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR15 Register Information (MA[5:0] = $0F_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Lower-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Lower-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[7:0] within a byte lane: 0_B: Do not invert 1_B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0]=55_H	1,2,3

Notes:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combi- nation of DQ's. Example: If MR15 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[7,6,5,3,1] will not be inverted, but the DQ Calibration patterns transmitted on DQ[4,2,0] will be inverted.
2. DMI[0] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3- OP[6].

Table 17 - MR15 Invert Register Pin Mapping

PIN	DQ0	DQ1	DQ2	DQ3	DMI0	DQ4	DQ5	DQ6	DQ7
MR15	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR16 Register Information (MA[5:0] = 10_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Bank Mask							

Function	Register Type	Operand	Data	Notes
Bank[7:0] Mask	Write-only	OP[7:0]	0_B: Bank Refresh enabled (default) : Unmasked 1_B: Bank Refresh disabled : Masked	1

OP[n]	Bank Mask	8-Bank SDRAM
0	xxxxxxx1	Bank 0
1	xxxxxx1x	Bank 1
2	xxxxx1xx	Bank 2
3	xxxx1xxx	Bank 3
4	xxx1xxxx	Bank 4
5	xx1xxxxx	Bank 5
6	x1xxxxxx	Bank 6
7	1xxxxxxx	Bank 7

Notes:
1. When a mask bit is asserted (OP[n]=1), refresh to that bank is disabled.
2. PASR bank-masking is on a per-channel basis. The two channels on the die may have different bank masking in dual channel devices.

MR17 Register Information (MA[5:0] = 11_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
PASR Segment Mask							

Function	Register Type	Operand	Data	Notes
PASR Segment Mask	Write-only	OP[7:0]	0_B: Segment Refresh enabled (default) 1_B: Segment Refresh disabled	

Segment	OP[n]	Segment Mask	2Gb per channel	3Gb per channel	4Gb per channel	6Gb per channel	8Gb per channel	12Gb per channel	16Gb per channel
			R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	R16:R14	R16:R14
0	0	xxxxxxx1	000_B						
1	1	xxxxxx1x	001_B						
2	2	xxxxx1xx	010_B						
3	3	xxxx1xxx	011_B						
4	4	xxx1xxxx	100_B						

Segment	OP[n]	Segment Mask	2Gb per channel	3Gb per channel	4Gb per channel	6Gb per channel	8Gb per channel	12Gb per channel	16Gb per channel
			R13:R11	R14:R12	R14:R12	R15:R13	R15:R13	R16:R14	R16:R14
5	5	xx1xxxxx	101_B						
6	6	x1xxxxxx	110_B	Not Allowed	110_B	Not Allowed	110_B	Not Allowed	110_B
7	7	1xxxxxxx	111_B		111_B		111_B		111_B

Notes:
1. This table indicates the range of row addresses in each masked segment. "X" is don't care for a particular seg- ment.
2. PASR segment-masking is on a per-channel basis. The two channels on the die may have different segment masking in dual channel devices.
3. For 3Gb, 6Gb, and 12Gb per channel densities, OP[7:6] must always be LOW (=00_B).

MR18 Register Information (MA[5:0] = 12_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - LSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0 - 255 LSB DRAM DQS Oscillator Count	1,2,3

Notes:
1. MR18 reports the LSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR19 Register Information (MA[5:0] = 13_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS Oscillator Count - MSB							

Function	Register Type	Operand	Data	Notes
DQS Oscillator (WR Training DQS Oscillator)	Read-only	OP[7:0]	0-255 MSB DRAM DQS Oscillator Count	1,2,3

Notes:
1. MR19 reports the MSB bits of the DRAM DQS Oscillator count. The DRAM DQS Oscillator count value is used to train DQS to the DQ data valid window. The value reported by the DRAM in this mode register can be used by the memory controller to periodically adjust the phase of DQS relative to DQ.
2. Both MR18 and MR19 must be read (MRR) and combined to get the value of the DQS Oscillator count.
3. A new MPC [Start DQS Oscillator] should be issued to reset the contents of MR18/MR19.

MR20 Register Information (MA[5:0] = 14_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Upper-Byte Invert Register for DQ Calibration							

Function	Register Type	Operand	Data	Notes
Upper-Byte Invert for DQ Calibration	Write-only	OP[7:0]	The following values may be written for any operand OP[7:0], and will be applied to the corresponding DQ locations DQ[15:8] within a byte lane: 0_B: Do not invert 1_B: Invert the DQ Calibration patterns in MR32 and MR40 Default value for OP[7:0] = 55_H	1,2

Notes:
1. This register will invert the DQ Calibration pattern found in MR32 and MR40 for any single DQ, or any combi- nation of DQ's. Example: If MR20 OP[7:0]=00010101B, then the DQ Calibration patterns transmitted on DQ[15,14,13,11,9] will not be inverted, but the DQ Calibration patterns transmitted on DQ[12,10,8] will be inverted.
2. DMI[1] is not inverted, and always transmits the "true" data contained in MR32/MR40.
3. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3- OP[6].

Table 18 - MR20 Invert Register Pin Mapping

PIN	DQ8	DQ9	DQ10	DQ11	DMI1	DQ12	DQ13	DQ14	DQ15
MR20	OP0	OP1	OP2	OP3	NO-Invert	OP4	OP5	OP6	OP7

MR22 Register Information (MA[5:0] = 16_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
RFU		ODTD-CA	ODTE-CS	ODTE-CK	SOC ODT		

MR22 Register Information for LPDDR4

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	000_B: Disable (Default) 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 111_B: RFU	1,2,3
ODTE-CK (CK ODT enabled for non-terminating rank)		OP[3]	0_B: ODT-CK Over-ride Disabled (Default) 1_B: ODT-CK Over-ride Enabled	2,3,4, 6,8
ODTE-CS (CS ODT enable for non-terminating rank)		OP[4]	0_B: ODT-CS Over-ride Disabled (Default) 1_B: ODT-CS Over-ride Enabled	2,3,5, 6,8
ODTD-CA (CA ODT termination disable)		OP[5]	0_B: ODT-CA Obeys ODT_CA bond pad (default) 1_B: ODT-CA Disabled	2,3,6, 7,8

Notes:
1. All values are “typical". Depend on SOC setting, value at disable grade may cause weak driver, user can set to other value if necessary.
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW com- mand to this MR

address, or read from with an MRR command to this address.

3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.
4. When OP[3]=1, then the CK signals will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CK is not, allowing CK to terminate on all DRAMs.
5. When OP[4]=1, then the CS signal will be terminated to the value set by MR11-OP[6:4] regardless of the state of the ODT_CA bond pad. This overrides the ODT_CA bond pad for configurations where CA is shared by two or more DRAMs but CS is not, allowing CS to terminate on all DRAMs.
6. For system configurations where the CK, CS, and CA signals are shared between packages, the package design should pro- vide for the ODT_CA ball to be bonded on the system board outside of the memory package. This provides the necessary control of the ODT function for all die with shared Command Bus signals.
7. When OP[5]=0, CA[5:0] will terminate when the ODT_CA bond pad is HIGH and MR11-OP[6:4] is VALID, and disables termination when ODT_CA is LOW or MR11-OP[6:4] is disabled. When OP[5]=1, termination for CA[5:0] is disabled, regardless of the state of the ODT_CA bond pad or MR11-OP[6:4].
8. To ensure proper operation in a multi-rank configuration, when CA, CK or CS ODT is enabled via MR11 OP[6:4] and also via MR22 or CA-ODT pad setting, the rank providing ODT will continue to terminate the command bus in all DRAM states including Active Self Refresh, Self Refresh Power-down, Active Power-down and Precharge Power-down.

MR22 Register Information for LPDDR4X

Function	Register Type	Operand	Data	Notes
SoC ODT (Controller ODT Value for VOH calibration)	Write-only	OP[2:0]	000_B: Disable (Default) 001_B: RZQ/1 (illegal if MR3 OP[0] = 0B) 010_B: RZQ/2 011_B: RZQ/3 (illegal if MR3 OP[0] = 0B) 100_B: RZQ/4 101_B: RZQ/5 (illegal if MR3 OP[0] = 0B) 110_B: RZQ/6 (illegal if MR3 OP[0] = 0B) 111_B: RFU	1,2,3
ODTE-CK (CK ODT enabled for non-terminating rank)		OP[3]	ODT bond PAD is ignored 0_B: ODT-CK Enable (Default) 1_B: ODT-CK Disable	2,3,4,
ODTE-CS (CS ODT enable for non-terminating rank)		OP[4]	ODT bond PAD is ignored 0_B: ODT-CS Enable (Default) 1_B: ODT-CS Disable	2,3,4
ODTD-CA (CA ODT termination disable)		OP[5]	ODT bond PAD is ignored 0_B: ODT-CA Enable (default) 1_B: ODT-CA Disable	2,3,4

Notes：

1. All values are “typical".
2. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. Only the registers for the set point determined by the state of the FSP-WR bit (MR13 OP[6]) will be written to with an MRW command to this MR address, or read from with an MRR command to this address.
3. There are two physical registers assigned to each bit of this MR parameter, designated set point 0 and set point 1. The device will operate only according to the values stored in the registers for the active set point, i.e., the set point determined by the state of the FSP-OP bit (MR13 OP[7]). The values in the registers for the inactive set point will be ignored by the device, and may be changed without affecting device operation.

MR23 Register Information (MA[5:0] = 17_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQS interval timer run time setting							

Function	Register Type	Operand	Data	Notes
DQS interval timer run time	Write-only	OP[7:0]	00000000_B: DQS interval timer stop via MPC Command (Default) 00000001_B: DQS timer stops automatically at 16^{th} clocks after timer start 00000010_B: DQS timer stops automatically at 32^{nd} clocks after timer start 00000011_B: DQS timer stops automatically at 48^{th} clocks after timer start 00000100_B: DQS timer stops automatically at 64^{th} clocks after timer start ---------- Thru ---------- 00111111_B: DQS timer stops automatically at $(63X16)^{th}$ clocks after timer start $01XXXXXX_B$: DQS timer stops automatically at 2048^{th} clocks after timer start $10XXXXXX_B$: DQS timer stops automatically at 4096^{th} clocks after timer start $11XXXXXX_B$: DQS timer stops automatically at 8192^{nd} clocks after timer start	1, 2

Notes:
1. MPC command with OP[6:0]=1001101_B (Stop DQS Interval Oscillator) stops DQS interval timer in case of MR23 OP[7:0] = 00000000_B.
2. MPC command with OP[6:0]=1001101_B (Stop DQS Interval Oscillator) is illegal with non-zero values in MR23 OP[7:0].

MR24 Register Information (MA[5:0] = 18_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
TRR Mode	TRR Mode BAn			Unlimited	MAC Value		

Function	Register Type	Operand	Data	Notes
MAC Value	Read-only	OP[2:0]	000_B: Unknown when bit OP3=0 (Note 1) Unlimited when bit OP3=1 (Note 2) 001_B: 700K 010_B: 600K 011_B: 500K 100_B: 400K 101_B: 300K 110_B: 200K 111_B: Reserved	
Unlimited MAC		OP[3]	0_B: OP[2:0] define MAC value 1_B: Unlimited MAC value (Note 2, Note 3)	

Function	Register Type	Operand	Data	Notes
TRR Mode BAn	Write-only	OP[6:4]	000_B: Bank 0 001_B: Bank 1 010_B: Bank 2 011_B: Bank 3 100_B: Bank 4 101_B: Bank 5 110_B: Bank 6 111_B: Bank 7	
TRR Mode		OP[7]	0_B: Disabled (default) 1_B: Enabled	

Notes:
1. Unknown means that the device is not tested for tMAC and pass/fail value in unknown.
2. There is no restriction to number of activates.
3. MR24 OP [2:0] is set to zero.

MR25 Register Information (MA[5:0] = 19_H)

Mode Register 25 contains one bit of readout per bank indicating that at least one resource is available for Post Package Repair programming.

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Bank7	Bank6	Bank5	Bank4	Bank3	Bank2	Bank1	Bank0

Function	Register Type	Operand	Data	Notes
PPR Resource	Read-only	OP[7:0]	0_B: PPR Resource is not available 1_B: PPR Resource is available	

MR30 Register Information (MA[5:0] = $1E_H$)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Valid 0 or 1							

Function	Register Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

Notes:
1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR32 Register Information (MA[5:0] = 20_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern “A” (default = $5A_H$)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write	OP[7:0]	X_B: An MPC command with OP[6:0]= 1000011_B causes the device to return the DQ Calibration Pattern contained in this register and (followed by) the contents of MR40. A default pattern "$5A_H$"is loaded at power-up or RESET, or the pattern may be overwritten with a MRW to this register. The contents of MR15 and MR20 will invert the data pattern for a given DQ (See MR15 for more information)	

MR33:38 Register Information (MA[5:0] = 21_H - 26_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Do not use							

MR39 Register Information (MA[5:0] = 27_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
Valid 0 or 1							

Function	Register Type	Operand	Data	Notes
SDRAM will ignore	Write-only	OP[7:0]	Don't care	1

Notes:
1. This register is reserved for testing purposes. The logical data values written to OP[7:0] shall have no effect on SDRAM operation, however timings need to be observed as for any other MR access command.

MR40 Register Information (MA[5:0] = 28_H)

OP[7]	OP[6]	OP[5]	OP[4]	OP[3]	OP[2]	OP[1]	OP[0]
DQ Calibration Pattern "B" (default = $3C_H$)							

Function	Register Type	Operand	Data	Notes
Return DQ Calibration Pattern MR32 + MR40	Write only	OP[7:0]	X_B: A default pattern "$3C_H$" is loaded at power- up or RESET, or the pattern may be overwritten with a MRW to this register. See MR32 for more information.	1,2,3

Notes:
1. The pattern contained in MR40 is concatenated to the end of MR32 and transmitted on DQ[15:0] and DMI[1:0] when DQ Read Calibration is initiated via a MPC command. The pattern transmitted serially on each data lane, organized "little endian" such that the low-order bit in a byte is transmitted first. If the data pattern in MR40 is 27_H , then the first bit transmitted with be a '1', followed by '1', '1', '0', '0', '1', '0', and '0'. The bit stream will be 00100111_B.
2. MR15 and MR20 may be used to invert the MR32/MR40 data patterns on the DQ pins. See MR15 and MR20 for more information. Data is never inverted on the DMI[1:0] pins.
3. The data pattern is not transmitted on the DMI[1:0] pins if DBI-RD is disabled via MR3-OP[6].
4. No Data Bus Inversion (DBI) function is enacted during DQ Read Calibration, even if DBI is enabled in MR3-OP[6].

1.10 Refresh Requirement

Between SRX command and SRE command, at least one extra refresh command is required. After the DRAM Self Refresh Exit command, in addition to the normal Refresh command at tREFI interval, the LPDDR4 DRAM requires minimum of one extra Refresh command prior to Self Refresh Entry command.

Table 19 - Refresh Requirement Parameters

Refresh Requirements		Symbol	2Gb	2Gb	4Gb	4Gb	8Gb	Units	Notes
Density per Channel			1Gb	2Gb		4Gb			
Number of banks per channel			8						
Refresh Window (tREFW) (TCASE ≤ 85°C)		tREFW	32					ms	
Refresh Window (tREFW) (1/2 Rate Refresh)		tREFW	16					ms	
Refresh Window (tREFW) (1/4 Rate Refresh)		tREFW	8					ms	
Required Number of REFRESH Commands in a tREFW window		R	8192					-	
Average Refresh Interval	REFAB	tREFI	3.904					us	
	REFPB	tREFIpb	488					ns	
Refresh Cycle Time (All Banks)		tRFCab	130			180		ns	
Refresh Cycle Time (Per Bank)		tRFCpb	60			90		ns	

Notes：

1. Refresh for each channel is independent of the other channel on the die, or other channels in a package. Power delivery in the user's system should be verified to make sure the DC operating conditions are maintained when multiple channels are refreshed simultaneously.
2. Self refresh abort feature is available for higher density devices starting with 12 Gb device and tXSR—abort(min) is defined as tRFCpb + 17.5ns.

2 Operating Conditions and Interface Specification

2.1 Absolute Maximum Ratings

Stresses greater than those listed may cause permanent damage to the device.
This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 20 - Absolute Maximum DC Ratings

Parameter	Symbol	Min	Max	Units	Notes
V_{DD1} supply voltage relative to Vss	V_{DD1}	-0.4	2.1	V	1
V_{DD2} supply voltage relative to Vss	V_{DD2}	-0.4	1.5	V	1
V_{DDQ} supply voltage relative to VSSQ	V_{DDQ}	-0.4	1.5	V	1
Voltage on any ball except V_{DD1} relative to Vss	VIN, VOUT	-0.4	1.5	V	
Storage Temperature	TSTG	-55	125	°C	2

Notes:
1. See "Power-Ramp" for relationships between power supplies.
2. Storage Temperature is the case surface temperature on the center/top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2.

2.2 AC and DC Operating Conditions

Table 21 - Recommended DC Operating Conditions

DRAM	Symbol	Min	Typ	Max	Unit	Notes
Core 1 Power	V_{DD1}	1.70	1.80	1.95	V	1,2
Core 2 Power/Input Buffer Power	V_{DD2}	1.06	1.10	1.17	V	1,2,3
I/O Buffer Power for LPDDR4	V_{DDQ}	1.06	1.10	1.17	V	2,3
I/O Buffer Power for LPDDR4X	V_{DDQ}	0.57	0.6	0.65	V	2,3

Notes:
1. V_{DD1} uses significantly less current than V_{DD2}.
2. The voltage range is for DC voltage only. DC is defined as the voltage supplied at the DRAM and is inclusive of all noise up to 20MHz at the DRAM package ball.
3. VdIVW and TdIVW limits described elsewhere in this document apply for voltage noise on supply voltages of up to 45 mV (peak-to-peak) from DC to 20MHz.

Table 22 - Input Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input Leakage current	I_L	-4	4	uA	1,2

Notes:
1. For CK_t，CK_c，CKE, CS, CA, ODT_CA and RESET_n. Any input 0V ≤ VIN ≤ V_{DD2} (All other pins not under test = 0V).
2. CA ODT is disabled for CK_t, CK_c, CS, and CA.

Table 23 - Input/Output Leakage Current

Parameter/Condition	Symbol	Min	Max	Unit	Notes
Input/Output Leakage current	I_{OZ}	-5	5	uA	1,2

Notes:
1. For DQ，DQS_t，DQS_c and DM I. Any I/O 0V ≤ VOUT≤ V_{DDQ}.
2. I/Os status are disabled: High Impedance and ODT Off.

Table 24 - Operating Temperature Range

Parameter/Condition	Symbol	Min	Max	Unit
Commercial	T_{OPER}	0	95	°C
Industrial		-40	95	°C
Automotive, A3		-40	95	°C
Automotive, A2		-40	105	°C

Note : Operating Temperature is the case surface temperature on the center-top side of the LPDDR4 device. For the measurement conditions, please refer to JESD51-2. See MR4 Register Information, and Refresh Requirement Parameter.

2.3 AC and DC Input/Output Measurement levels

2.3.1 1.1 V High speed LVCMOS (HS_LLVCMOS)

This section defines power supply voltage range, dc interface, switching parameter and overshoot/undershoot for high speed lower low-voltage CMOS family of non-terminated digital circuits. The specifications in this section represent a minimum set of interface specifications for CMOS compatible circuits. The purpose of this section is to provide a standard of specification for uniformity, multiplicity of sources, elimination of confusion, and ease of device specification and design by users.

2.3.1.1 Standard specifications

All voltages are referenced to ground except where noted.

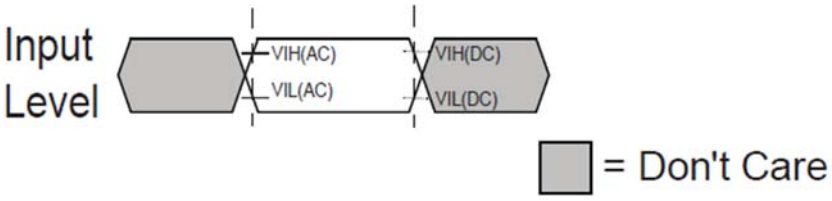
2.3.1.2 Input Levels for CKE

Table 25 – Input Levels for CKE

Parameter	Symbol	Min	Max	Unit	Note
Input high level (AC)	VIH(AC)	0.75*V_{DD2}(or V_{DDQ})	V_{DD2} (or V_{DDQ})+0.2	V	1
Input low level (AC)	VIL(AC)	-0.2	0.25* V_{DD2}(or V_{DDQ})	V	1
Input high level (DC)	VIH(DC)	0.65* V_{DD2}(or V_{DDQ})	V_{DD2}(or V_{DDQ})+0.2	V	
Input low level (DC)	VIL(DC)	-0.2	0.35* V_{DD2}(or VDDQ)	V	

Note 1: See the AC Over/Undershoot section

Figure 6 - Input Timing Definition for CKE



Notes:
1. AC level is guaranteed transition point.
2. DC level is hysteresis.

2.3.1.3 Input Levels for Reset_n and ODT_CA

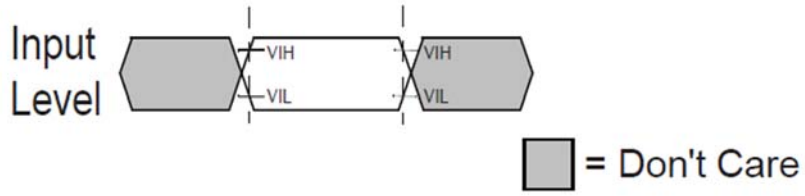
This definition applies to Reset_n and ODT_CA. Table 26 provides the input level. Figure 7 shows the timing.

Table 26 – Input Levels for Reset_n and ODT_CA

Parameter	Symbol	Min	Max	Unit	Note
Input high level	VIH	0.80*V_{DD2}	V_{DD2}+0.2	V	1
Input low level	VIL	-0.2	0.20*V_{DD2}	V	1

Note 1: See the AC Over/Undershoot section

Figure 7 - Input AC Timing Definition for Reset_n and ODT_CA



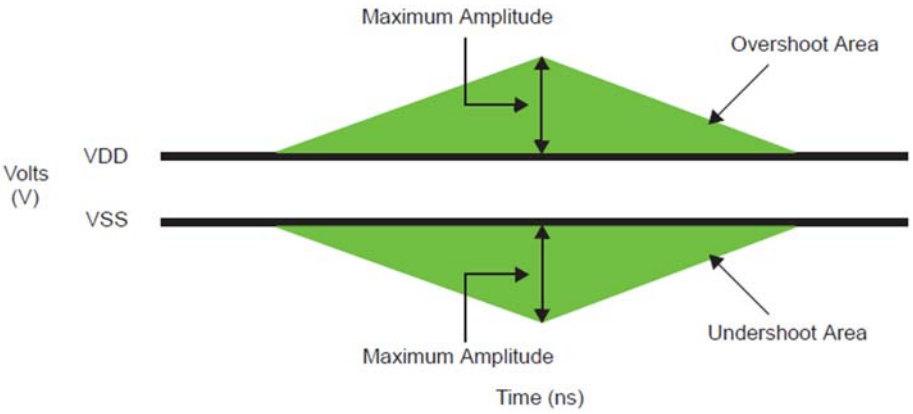
2.3.1.4 AC Over/Undershoot

2.3.1.4.1 LPDDR4 AC Over/Undershoot

Table 27 – LPDDR4 AC Over/Undershoot

Parameter	Specification
Maximum peak Amplitude allowed for overshoot	0.35V
Maximum peak Amplitude allowed for undershoot area	0.35V
Maximum overshoot area above VDD/VDDQ	0.8V-ns
Maximum undershoot area below VSS/VSSQ	0.8V-ns

Figure 8 - AC Overshoot and Undershoot Definition for Address and Control Pins



2.3.2 Differential Input Voltage

2.3.2.1 Differential Input Voltage for CK

The minimum input voltage need to satisfy both Vindiff_CK and Vindiff_CK /2 specification at input receiver and their measurement period is 1tCK. Vindiff_CK is the peak to peak voltage centered on 0 volts differential and Vindiff_CK /2 is max and min peak voltage from 0V.

Figure 9 - CK Differential Input Voltage

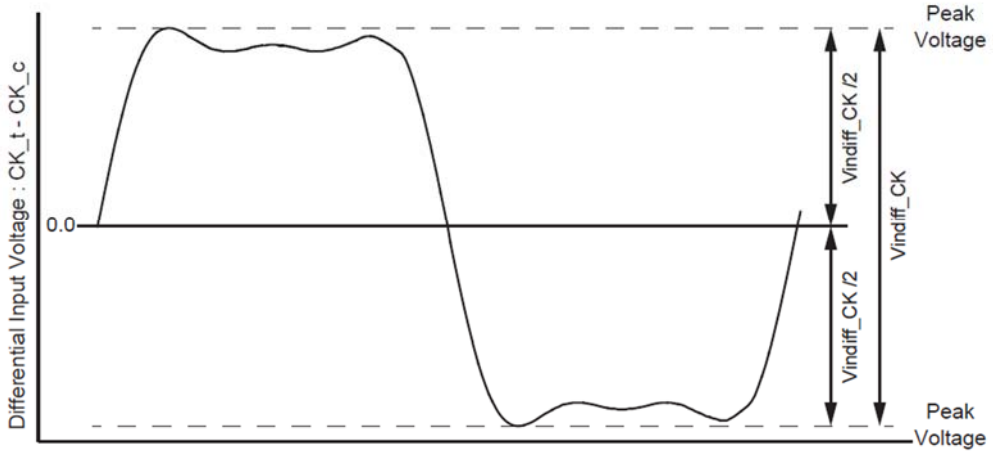


Table 28 – CK differential input voltage

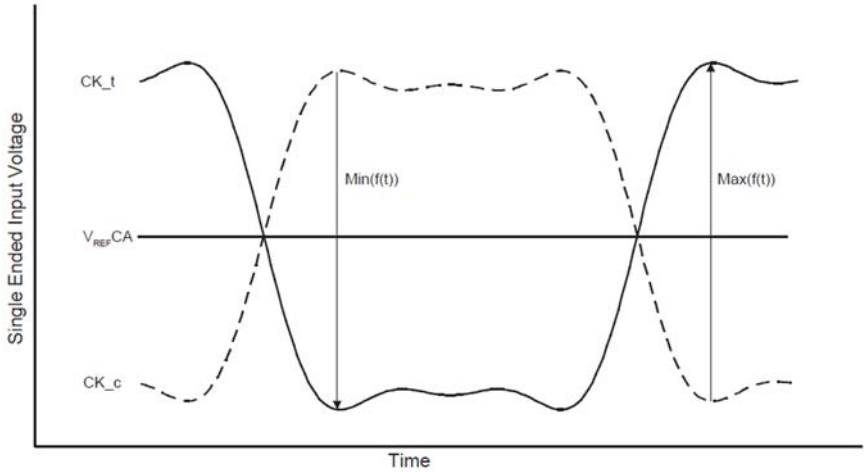
Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
CK differential input voltage	Vindiff_CK	420	-	380	-	360	-	mV	1,2

Notes:
1. These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.
2. The peak voltage of Differential CK signals is calculated in a following equation.
   Vindiff_CK = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VCK_t - VCK_c

2.3.2.2 Peak voltage calculation method

The peak voltage of Differential Clock signals are calculated in the following equation (see Figure 10).
VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VCK_t - VCK_c

Figure 10 - Definition of differential Clock Peak Voltage

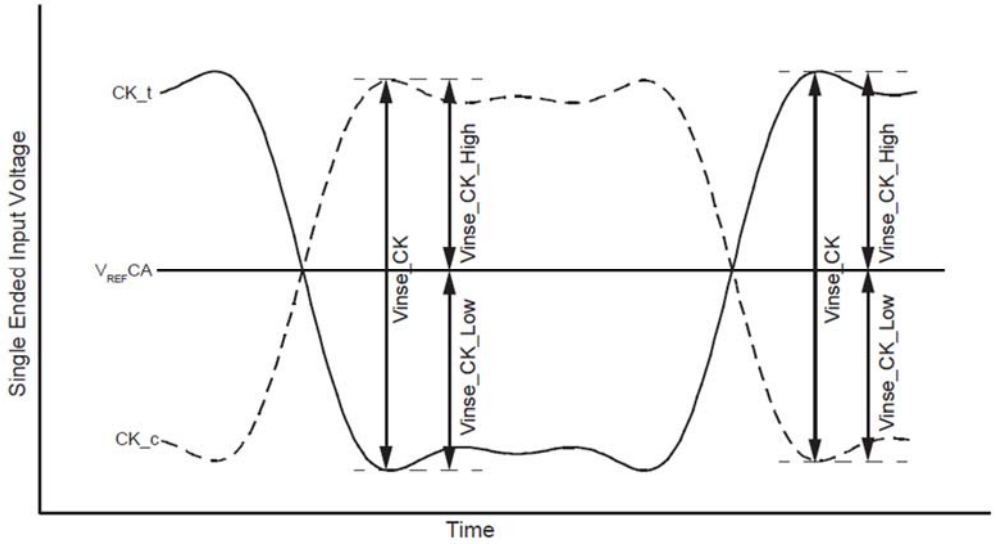


Notes: 1. $V_{REF}CA$ is LPDDR4 SDRAM internal setting value by V_{REF} Training.

2.3.2.3 Single-Ended Input Voltage for Clock

The minimum input voltage needs to satisfy both Vinse_CK, Vinse_CK_High/Low specification at input receiver.

Figure 11 - Clock Single-Ended Input Voltage



Notes: 1. V_{REF}CA is LPDDR4 SDRAM internal setting value by V_{REF} Training.

Table 29 – Clock Single-Ended input voltage

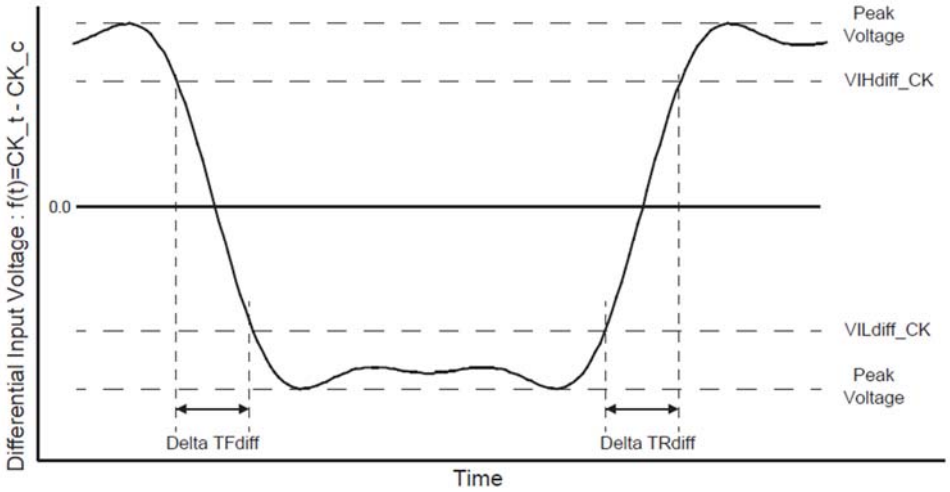
Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Clock Single-Ended input voltage	Vinse_CK	210	-	190	-	180	-	mV	1
Clock Single-Ended input voltage High from VREFCA	Vinse_CK_High	105	-	95	-	90	-	mV	1
Clock Single-Ended input voltage Low from VREFCA	Vinse_CK_Low	105	-	95	-	90	-	mV	1

Note 1: These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

2.3.2.4 Differential Input Slew Rate Definition for Clock

Input slew rate for differential signals (CK_t, CK_c) are defined and measured as shown in Figure 12 and Table 30 through Table 32.

Figure 12 - Differential Input Slew Rate Definition for CK_t, CK_c



Notes: 1. Differential signal rising edge from VILdiff_CK to VIHdiff_CK must be monotonic slope.
2. Differential signal falling edge from VIHdiff_CK to VILdiff_CK must be monotonic slope.

Table 30 – Differential Input Slew Rate Definition for CK_t, CK_c

Description	From	To	Defined by
Differential input slew rate for rising edge(CK_t - CK_c)	VILdiff_CK	VIHdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTRdiff
Differential input slew rate for falling edge(CK_t - CK_c)	VIHdiff_CK	VILdiff_CK	|VILdiff_CK - VIHdiff_CK|/DeltaTFdiff

Table 31 – Differential Input Level for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input High	VIHdiff_CK	175	-	155	-	145	-	mV	1
Differential Input Low	VILdiff_CK	-	-175	-	-155	-	-145	mV	1

Note 1: These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column 1600/1867.

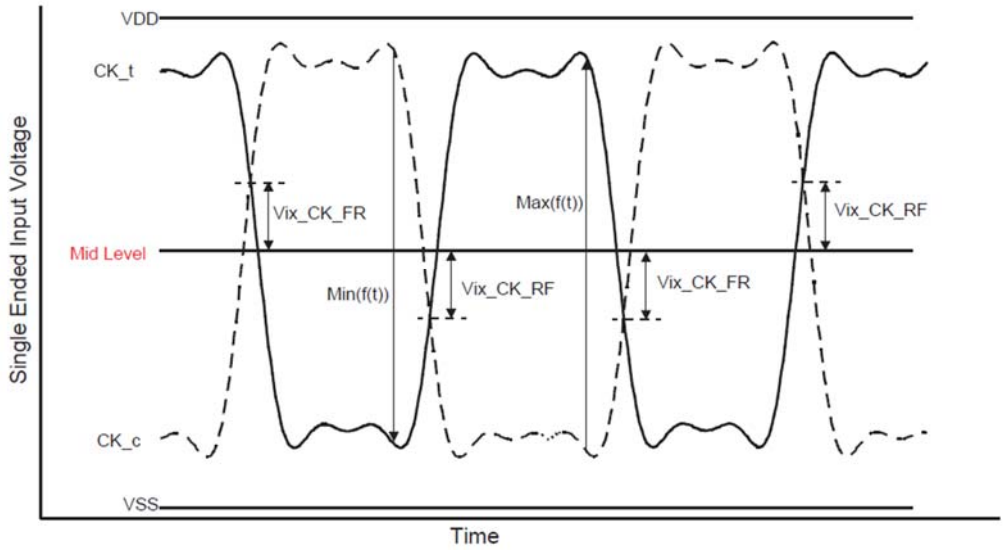
Table 32 – Differential Input Slew Rate for CK_t, CK_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for Clock	SRIdiff_CK	2	14	2	14	2	14	V/ns	

2.3.2.5 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (CK_t, CK_c) are shown in Figure 13 and must meet the requirements in Table 33. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level.

Figure 13 - Vix Definition (Clock)



Notes: 1. The base level of Vix_CK_FR/RF is V_{REF}CA that is LPDDR4 SDRAM internal setting value by V_{REF} Training.

Table 33 – Cross point voltage for differential input signals (Clock)

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Clock Differential input cross point voltage ratio	Vix_CK_ratio	-	25	-	25	-	25	%	1,2,3, 4,5

Notes:
1. These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column,1600/1867.
2. Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_FR/|Min(f(t))|
3. Vix_CK_Ratio is defined by this equation: Vix_CK_Ratio = Vix_CK_RF/Max(f(t))
4. Vix_CK_FR is defined as delta between cross point (CK_t fall, CK_c rise) to Min(f(t))/2.
   Vix_CK_RF is defined as delta between cross point (CK_t rise, CK_c fall) to Max(f(t))/2.
5. In LPDDR4X un-terminated case, CK mid-level is calculated as:
   High level = VDDQ, Low level=VSS, Mid-level = VDDQ/2.
   In LPDDR4 un-terminated case, Mid-level must be equal or lower than 369mV (33.6% of VDD2).

2.3.2.6 Differential Input Voltage for DQS

The minimum input voltage need to satisfy both Vindiff_DQS and Vindiff_DQS /2 specification at input receiver and their measurement period is 1UI(tCK/2). Vindiff_DQS is the peak to peak voltage centered on 0 volts differential and Vindiff_DQS /2 is max and min peak voltage from 0V.

Figure 14 - DQS Differential Input Voltage

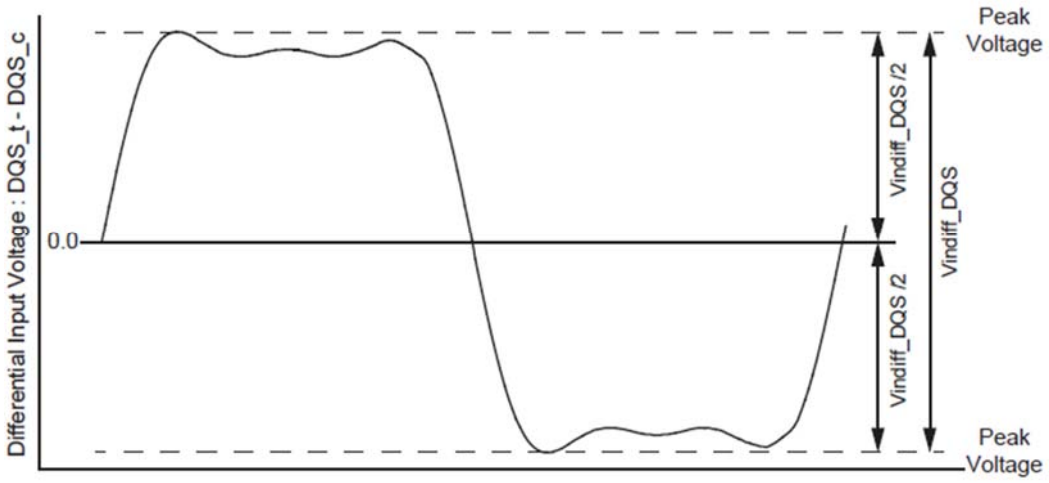


Table 34 – DQS differential input voltage

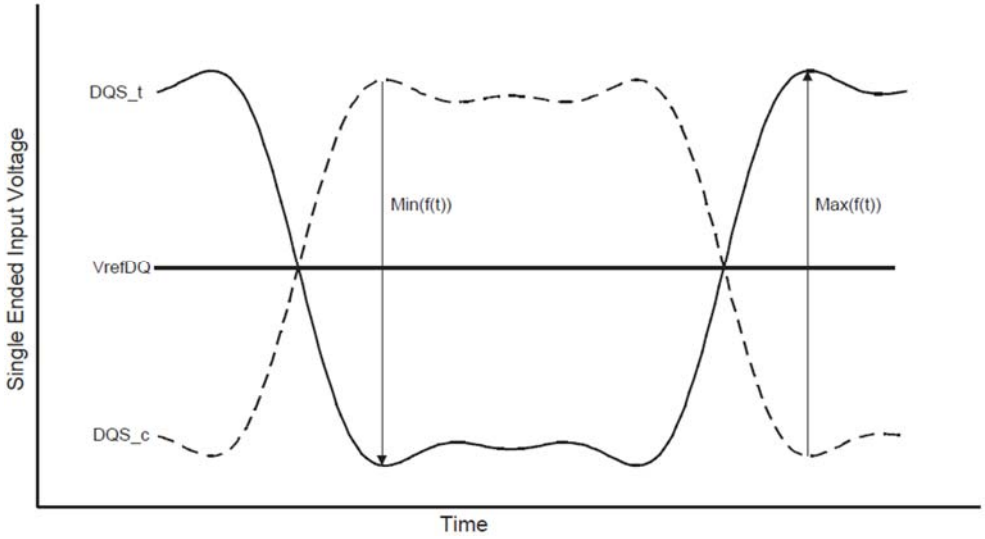
Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS differential input	Vindiff_DQS	360	-	360	-	340	-	mV	1,2

Notes
1. These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column,1600/1867.
2. The peak voltage of Differential DQS signals is calculated in a following equation.
   Vindiff_DQS = (Max Peak Voltage) - (Min Peak Voltage)
   Max Peak Voltage = Max(f(t))
   Min Peak Voltage = Min(f(t))
   f(t) = VDQS_t - VDQS_c

2.3.2.7 Peak voltage calculation method

The peak voltage of Differential DQS signals, shown in Figure 15, are calculated in a following equation.
VIH.DIFF.Peak Voltage = Max(f(t))
VIL.DIFF.Peak Voltage = Min(f(t))
f(t) = VDQS_t - VDQS_c

Figure 15 - Definition of differential DQS Peak Voltage

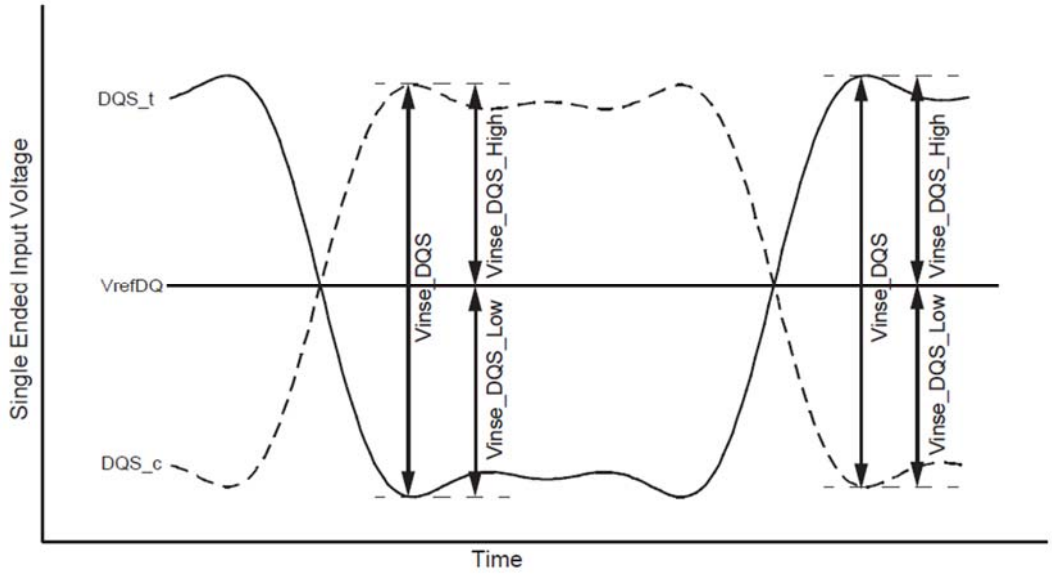


Notes: 1. VrefDQ is LPDDR4 SDRAM internal setting value by Vref Training.

2.3.2.8 Single-Ended Input Voltage for DQS

The minimum input voltage need to satisfy both Vinse_DQS, Vinse_DQS_High/Low specification at input receiver, as shown in Figure 16 and Table 35.

Figure 16 - DQS Single-Ended Input Voltage



Notes : 1. VrefDQ is LPDDR4 SDRAM internal setting value by Vref Training.

Table 35 – DQS Single-Ended input voltage

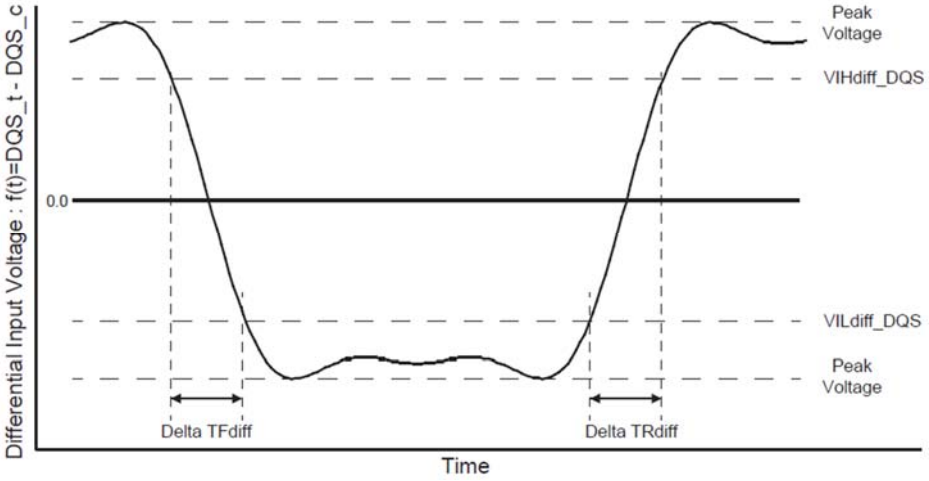
Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS Single-Ended input voltage	Vinse_DQS	180	-	180	-	170	-	mV	1
DQS Single-Ended input voltage High from VREFDQ	Vinse_DQS_High	90	-	90	-	85	-	mV	1
DQS Single-Ended input voltage Low from VREFDQ	Vinse_DQS_Low	90	-	90	-	85	-	mV	1

Note 1: These requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column,1600/1867.

2.3.2.9 Differential Input Slew Rate Definition for DQS

Input slew rate for differential signals (DQS_t, DQS_c) are defined and measured as shown in Figure 17 and Table 36 to Table 38.

Figure 17 - Differential Input Slew Rate Definition for DQS_t, DQS_c



Notes :
1. Differential signal rising edge from VILdiff_DQS to VIHdiff_DQS must be monotonic slope.
2. Differential signal falling edge from VIHdiff_DQS to VILdiff_DQS must be monotonic slope.

Table 36 – Differential Input Slew Rate Definition for DQS_t, DQS_c

Description	From	To	Defined by
Differential input slew rate for rising edge(DQS_t - DQS_c)	VILdiff_DQS	VIHdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/DeltaTRdiff
Differential input slew rate for falling edge(DQS_t - DQS_c)	VIHdiff_DQS	VILdiff_DQS	|VILdiff_DQS - VIHdiff_DQS|/DeltaTFdiff

Table 37 – Differential Input Level for DQS_t, DQS_c

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input High	VIHdiff_DQS	140	-	140	-	120	-	mV	1
Differential Input Low	VILdiff_DQS	-	-140	-	-140	-	-120	mV	1

Note 1: The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.

Table 38 – Differential Input Slew Rate for DQS_t, DQS_c

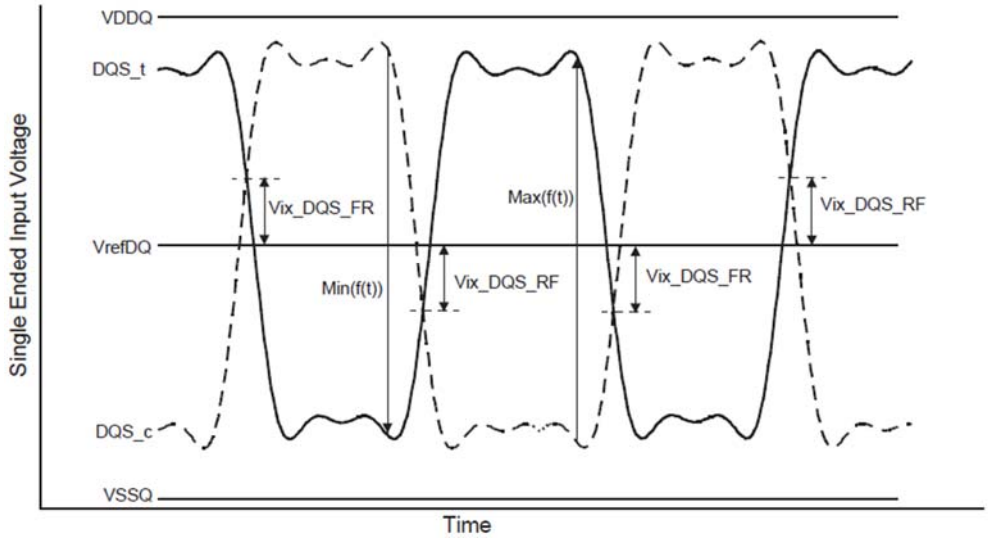
Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
Differential Input Slew Rate for Clock	SRIdiff	2	14	2	14	2	14	V/ns	1

Note 1: The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.

2.3.2.10 Differential Input Cross Point Voltage

The cross point voltage of differential input signals (DQS_t, DQS_c) must meet the requirements in Table 39. The differential input cross point voltage VIX is measured from the actual cross point of true and complement signals to the mid level that is VREFDQ, as shown in Figure 18.

Figure 18 - Vix Definition (DQS)



Notes : 1. The base level of Vix_DQS_FR/RF is VrefDQ that is LPDDR4 SDRAM internal setting value by Vref Training.

Table 39 – Cross point voltage for differential input signals (DQS)

Parameter	Symbol	Data Rate						Unit	Note
		1600/1867		2133/2400/3200		3733/4266			
		Min	Max	Min	Max	Min	Max		
DQS Differential input cross point voltage ratio	Vix_DQS_ratio	-	20	-	20	-	20	%	1,2,3

Notes:
1. The following requirements apply for DQ operating frequencies at or below 1333Mbps for all speed bins for the first column, 1600/1867.
2. Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_FR/|Min(f(t))|.
3. Vix_DQS_Ratio is defined by this equation: Vix_DQS_Ratio = Vix_DQS_RF/Max(f(t))

2.3.3 AC/DC Input level for ODT input

Table 40 – LPDDR4 Input Level for ODT

Symbol		Min	Max	Unit	Note
VIHODT	ODT Input High Level	0.75*V_{DD2}	V_{DD2}+0.2	V	1
VILODT	ODT Input Low Level	-0.2	0.25*V_{DD2}	V	1

Note 1: See Overshoot and Undershoot Specifications in Table 45.

2.3.4 Single Ended Output Slew Rate

Figure 19 - Single Ended Output Slew Rate Definition

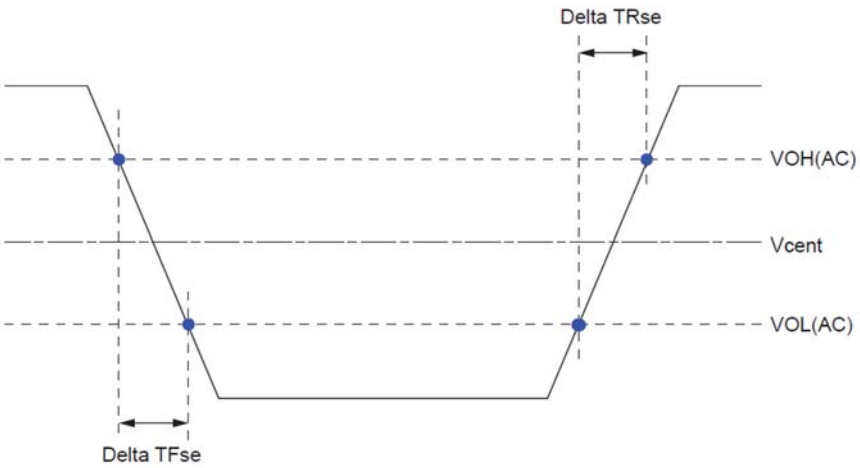


Table 41 – Output Slew Rate (single-ended) for LPDDR4

Parameter	Symbol	Value		Unit
		Min[1]	Max[2]	
Single-ended Output Slew Rate (VOH = VDDQ/3)	SRQse	3.5	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-

Table 42 – Output Slew Rate (single-ended) for LPDDR4X

Parameter	Symbol	Value		Unit
		Min[1]	Max[2]	
Single-ended Output Slew Rate (VOH = VDDQ*0.5)	SRQse	3.0	9	V/ns
Output slew-rate matching Ratio (Rise to Fall)	-	0.8	1.2	-

Notes:
1. Description:
   SR: Slew Rate
   Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
   se: Single-ended Signals
2. Measured with output reference load.
3. The ratio of pull-up to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.
4. The output slew rate for falling and rising edges is defined and measured between VOL(AC)=0.2*VOH(DC) and VOH(AC)= 0.8*VOH(DC).
5. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

2.3.5 Differential Output Slew Rate

Figure 20 - Differential Output Slew Rate Definition

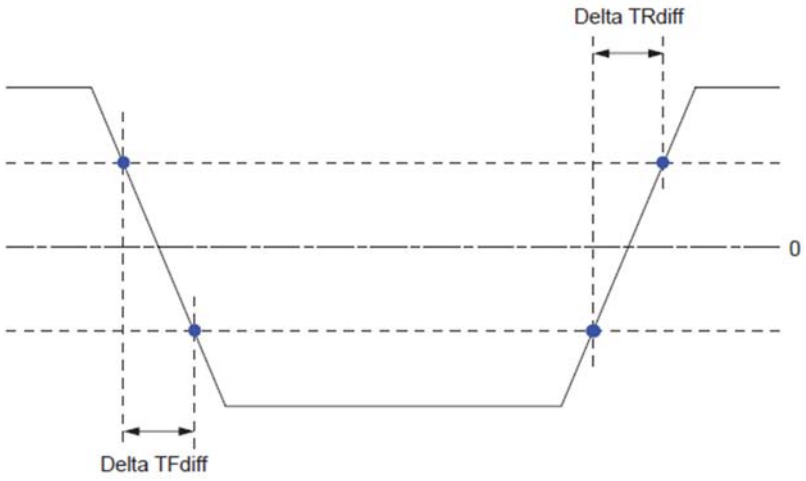


Table 43 – Differential Output Slew Rate for LPDDR4

Parameter	Symbol	Value		Unit
		Min	Max	
Differential Output Slew Rate (VOH = VDDQ/3)	SRQdiff	7	18	V/ns

Table 44 – Differential Output Slew Rate for LPDDR4X

Parameter	Symbol	Value		Unit
		Min	Max	
Differential Output Slew Rate (VOH = VDDQ*0.5)	SRQdiff	6	18	V/ns

Notes:
1. Description:
   SR: Slew Rate
   Q: Query Output (like in DQ, which stands for Data-in, Query-Output)
   diff: Differential Signals
2. Measured with output reference load.
3. The output slew rate for falling and rising edges is defined and measured between VOL(AC)= -0.8*VOH(DC) and VOH(AC)= 0.8*VOH(DC).
4. Slew rates are measured under average SSO conditions, with 50% of DQ signals per data byte switching.

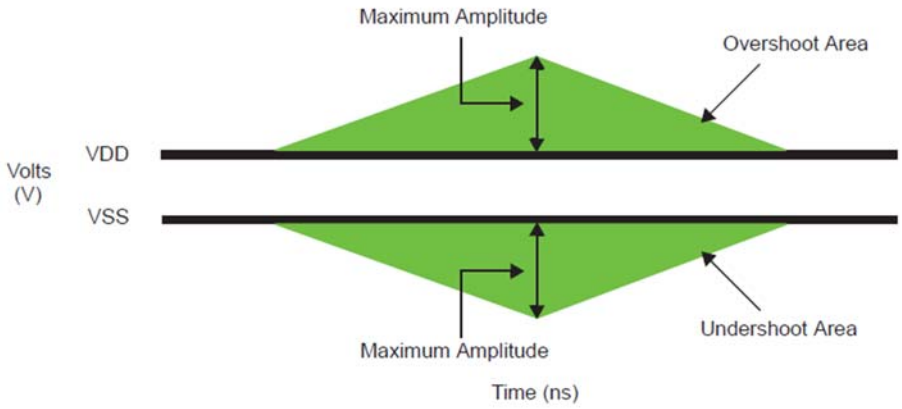
2.3.6 Overshoot and Undershoot for LVSTL

Table 45 – AC Overshoot/Undershoot Specification

Parameter		Data Rate				Unit
		1600	1866	3200	4266	
Maximum peak amplitude allowed for overshoot area.	Max	0.3	0.3	0.3	0.3	V
Maximum peak amplitude allowed for undershoot area.	Max	0.3	0.3	0.3	0.3	V
Maximum area above VDD.	Max	0.1	0.1	0.1	0.1	V-ns
Maximum area below VSS.	Max	0.1	0.1	0.1	0.1	V-ns

Notes:
1. VDD2 stands for VDD for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VDD stands for VDDQ for DQ, DMI, DQS_t and DQS_c.
2. VSS stands for VSS for CA[5:0], CK_t, CK_c, CS_n, CKE and ODT. VSS stands for VSSQ for DQ, DMI, DQS_t and DQS_c.
3. Maximum peak amplitude values are referenced from actual VDD and VSS values.
4. Maximum area values are referenced from maximum operating VDD and VSS values.

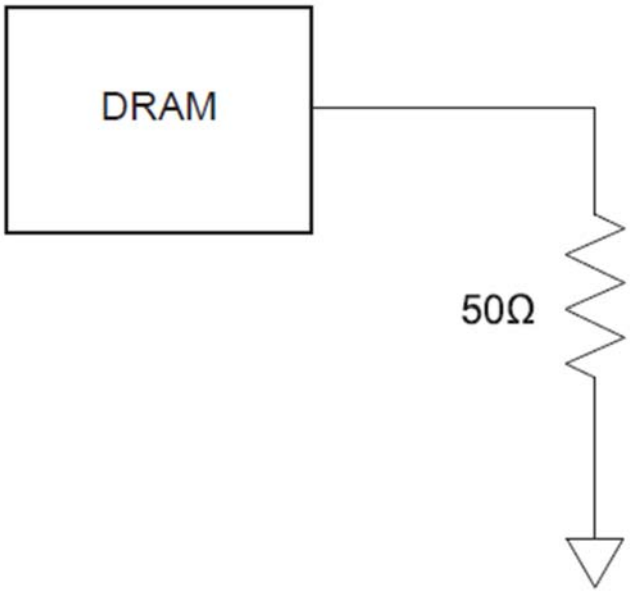
Figure 21 - Overshoot and Undershoot Definition



2.3.7 LPDDR4 Driver Output Timing Reference load

These 'Timing Reference Loads' are not intended as a precise representation of any particular system environment or a depiction of the actual load presented by a production tester. System designers should use IBIS or other simulation tools to correlate the timing reference load to a system environment. Manufacturers correlate to their production test conditions, generally one or more coaxial transmission lines terminated at the tester electronics.

Figure 22 - Driver Output Reference Load for Timing and Slew Rate

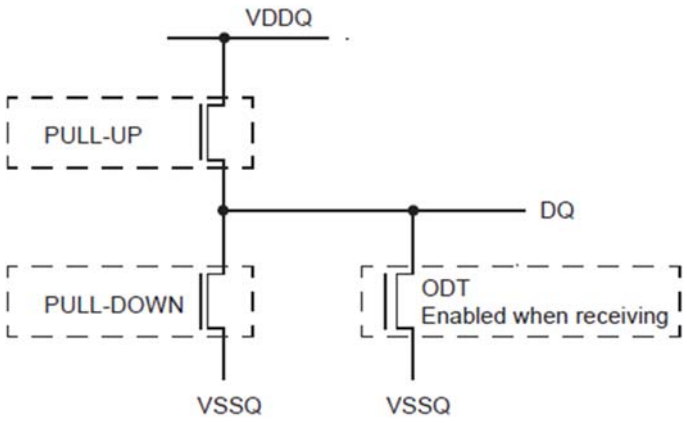


Notes: 1. All output timing parameter values are reported with respect to this reference load.

2.3.8 LVSTL(Low Voltage Swing Terminated Logic) IO System

LVSTL I/O cell is comprised of pull-up, pull-down dirver and a terminator. The basic cell is shown in Figure 23.

Figure 23 - LVSTL I/O Cell

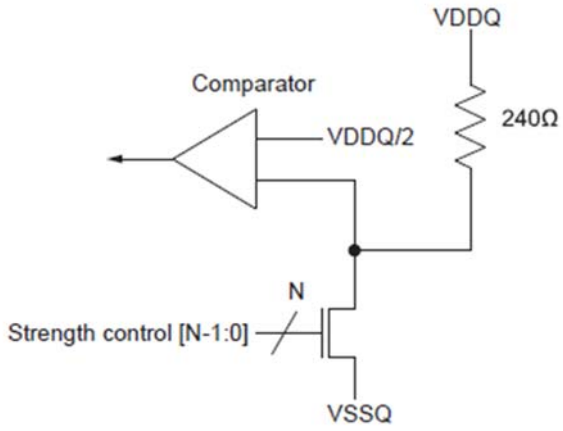


To ensure that the target impedance is achived the LVSTL I/O cell is designed to calibrated as below procedure.

1. First calibrate the pull-down device against a 240 Ω resister to VDDQ via the ZQ pin.

   • Set Strength Control to minimum setting.
   • Increase drive strength until comparator detects data bit is less than VDDQ/2.
   • NMOS pull-down device is calibrated to 240 Ω.

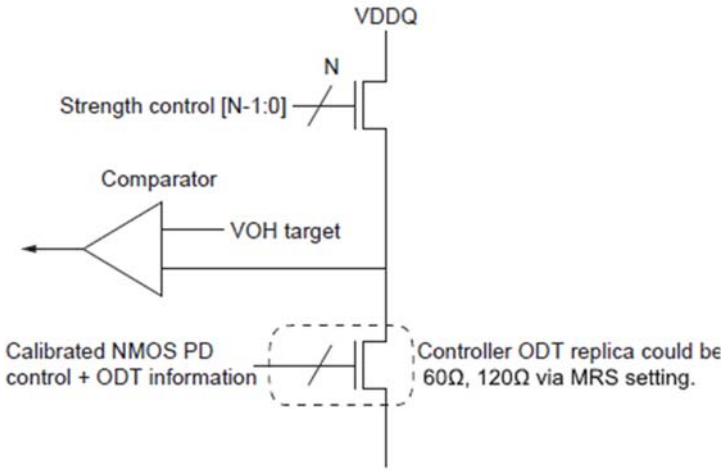
Figure 24 - Pull-down calibration



2. Then calibrate the pull-up device against the calibrated pull-down device.

   • Set VOH target and NMOS controller ODT replica via MRS (VOH can be automatically controlled by ODT MRS).
   • Set Strength Control to minimum setting.
   • Increase drive strength until comparator detects data bit is grater than VOH target.
   • NMOS pull-up device is now calibrated to VOH target.

Figure 25 - Pull-up calibration



2.4 Output Driver and Termination Register Temperature and Voltage Sensitivity

If temperature and/or voltage change after calibration, the tolerance limits widen according to the Table 46, Table 47 and Table 48.

Table 46 – Output Driver and Termination Register Sensitivity Definition for LPDDR4

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	0.33 x V_{DDQ}	90-(dRondT x |ΔT|)-(dRondV x |ΔV|)	110+(dRondT x |ΔT|)+(dRondV x |ΔV|)	%	1,2
VOH_{PU}	0.33 x V_{DDQ}	90-(dVOHdT x |ΔT|)-(dVOHdV x |ΔV|)	110+(dVOHdT x |ΔT|)+(dVOHdV x |ΔV|)	%	1,2,5
$R_{TT(I/O)}$	0.33 x V_{DDQ}	90-(dRondT x |ΔT|)-(dRondV x |ΔV|)	110+(dRondT x |ΔT|)+(dRondV x |ΔV|)	%	1,2,3
$R_{TT(In)}$	0.33 x V_{DD2}	90-(dRondT x |ΔT|)-(dRondV x |ΔV|)	110+(dRondT x |ΔT|)+(dRondV x |ΔV|)	%	1,2,4

Notes：
1. ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration).
2. $dR_{ON}dT$, $dR_{ON}dV$, dVOHdT, dVOHdV, $dR_{TT}dV$, and $dR_{TT}dT$ are not subject to production test but are verified by design and characterization.
3. This parameter applies to Input/Output pin such as DQS, DQ and DMI.
4. This parameter applies to Input pin such as CK, CA and CS.
5. Refer to 4.39 Pull Up/Pull Down Driver Characteristics for VOH_{PU}.

Table 47 – Output Driver and Termination Register Sensitivity Definition for LPDDR4X

Resistor	Definition Point	Min	Max	Unit	Notes
R_{ONPD}	0.50 x V_{DDQ}	90-(dRondT x |ΔT|)-(dRondV x |ΔV|)	110+(dRondT x |ΔT|)+(dRondV x |ΔV|)	%	1,2
VOH_{PU}	0.50 x V_{DDQ}	90-(dVOHdT x |ΔT|)-(dVOHdV x |ΔV|)	110+(dVOHdT x |ΔT|)+(dVOHdV x |ΔV|)	%	1,2,5
$R_{TT(I/O)}$	0.50 x V_{DDQ}	90-(dRondT x |ΔT|)-(dRondV x |ΔV|)	110+(dRondT x |ΔT|)+(dRondV x |ΔV|)	%	1,2,3
$R_{TT(In)}$	0.50 x V_{DDQ}	90-(dRondT x |ΔT|)-(dRondV x |ΔV|)	110+(dRondT x |ΔT|)+(dRondV x |ΔV|)	%	1,2,4

Notes：
1. ΔT = T - T(@ Calibration), ΔV = V - V(@ Calibration).
2. $dR_{ON}dT$, $dR_{ON}dV$, dVOHdT, dVOHdV, $dR_{TT}dV$, and $dR_{TT}dT$ are not subject to production test but are verified by design and characterization.
3. This parameter applies to Input/Output pin such as DQS, DQ and DMI.
4. This parameter applies to Input pin such as CK, CA and CS.
5. Refer to 4.39 Pull Up/Pull Down Driver Characteristics for VOH_{PU}.

Table 48 – Output Driver and Termination Register Temperature and Voltage Sensitivity

Symbol	Parameter	Min	Max	Unit
dRONdT	RON Temperature Sensitivity	0.00	0.75	%/°C
dRONdV	RON Voltage Sensitivity	0.00	0.20	%/mV
dVOHdT	VOH Temperature Sensitivity	0.00	0.75	%/°C
dVOHdV	VOH Voltage Sensitivity	0.00	0.35	%/mV
dRTTdT	RTT Temperature Sensitivity	0.00	0.75	%/°C
dRTTdV	RTT Voltage Sensitivity	0.00	0.20	%/mV

2.5 Interface Capacitance

Table 49 – Input/output capacitance

Parameter	Symbol		Value	Units	Notes
Input capacitance, CK_t and CK_c	CCK	Min	0.5	pF	1,2
		Max	0.9		
Input capacitance delta, CK_t and CK_c	CDCK	Min	0.0	pF	1,2,3
		Max	0.09		
Input capacitance, All other input-only pins	CI	Min	0.5	pF	1,2,4
		Max	0.9		
Input capacitance delta, All other input-only pins	CDI	Min	-0.1	pF	1,2,5
		Max	0.1		
Input/output capacitance, DQ, DMI, DQS_t, DQS_c	CIO	Min	0.7	pF	1,2,6
		Max	1.3		
Input/output capacitance delta, DQS_t,DQS_c	CDDQS	Min	0.0	pF	1,2,7
		Max	0.1		
Input/output capacitance delta, DQ, DMI	CDIO	Min	-0.1	pF	1,2,8
		Max	0.1		
Input/output capacitance, ZQ pin	CZQ	Min	0.0	pF	1,2
		Max	5.0		

Notes:

1. This parameter applies to die device only (does not include package capacitance).
2. This parameter is not subject to production test. It is verified by design and characterization. The capacitance is measured according to JEP147 (Procedure for measuring input capacitance using a vector network analyzer (VNA) with V_{DD1}, V_{DD2}, V_{DDQ}, VSS, VSSQ applied and all other pins floating.
3. Absolute value of CCK_ t, CCK_ c.
4. CI applieds to CS_n, CKE, CA0~CA5.
5. CDI = CI - 0.5 * (CCK_t + CCK_c)
6. DMI loading matches DQ and DQS.
7. Absolute value of CDQS_t and CDQS_c.
8. CDIO = CIO - 0.5 * (CDQS_t + CDQS_c) in byte-lane.

3 Speed Bins, AC Timing and IDD

3.1 Speed Bins

Table 50 – Read and Write Latencies

Read Latency		Write Latency		nWR	nRTP	Lower Clock Frequency Limit [MHz]	Upper Clock Frequency Limit [MHz]	Notes
No DBI	w/DBI	Set A	Set B			(>)	(≤)	
6	6	4	4	6	8	10	266	1,2,3,4 ,5,6
10	12	6	8	10	8	266	533	
14	16	8	2	16	8	533	800	
20	22	10	18	20	8	800	1066	
24	28	12	22	24	10	1066	1333	
28	32	14	26	30	12	1333	1600	
32	36	16	30	34	14	1600	1866	
36	40	18	34	40	16	1866	2133	

Notes:

1. The LPDDR4 SDRAM device should not be operated at a frequency above the Upper Frequency Limit, or below the Lower Frequency Limit, shown for each RL, WL, nRTP, or nWR value.
2. DBI for Read operations is enabled in MR3 OP[6]. When MR3 OP[6]=0, then the "No DBI" column should be used for Read Latency. When MR3 OP[6]=1, then the "w/DBI" column should be used for Read Latency.
3. Write Latency Set “A” and Set "B" is determined by MR2 OP[6]. When MR2 OP[6]=0, then Write Latency Set "A" should be used. When MR2 OP[6]=1，then Write Latency Set "B" should be used.
4. The programmed value of nWR is the number of clock cycles the LPDDR4 SDRAM device uses to determine the starting point of an internal Precharge operation after a Write burst with AP (Auto Pre- charge). It is determined by RU(tWR/tCK).
5. The programmed value of nRTP is the number of clock cycles the LPDDR4 SDRAM device uses to determine the starting point of an internal Precharge operation after a Read burst with AP (Auto Pre- charge). It is determined by RU(tRTP/tCK).
6. nRTP shown in this table is valid for BL16 only. For BL32, the SDRAM will add 8 clocks to the nRTP value before starting a precharge.

The ODT Mode is enabled if MR11 OP[3:0] are non-zero. In this case, the value of RTT is determined by the settings of those bits.
The ODT Mode is disabled if MR11 OP[3] = 0.

Table 51 – ODTLon and ODTLoff Latency

ODTLon Latency[1] tWPRE = 2tCK		ODTLoff Latency[2]		Lower Clock Frequency Limit[MHz]	Upper Clock Frequency Limit[MHz]
WL Set “A"	WL Set "B"	WL Set "A"	WL Set "B"	(>)	(≤)
N/A	N/A	N/A	N/A	10	266
N/A	N/A	N/A	N/A	266	533
N/A	6	N/A	22	533	800
4	12	20	28	800	1066
4	14	22	32	1066	1333
6	18	24	36	1333	1600
6	20	26	40	1600	1866
8	24	28	44	1866	2133

Notes:

1. ODTLon is referenced from CAS-2 command.
2. ODTLoff as shown in table assumes BL=16. For BL32, 8 tCK should be added.

3.2 AC Timing

Table 52 – Clock AC Timing

Parameter	Symbol	LPDDR4-3200		LPDDR4-3733		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max		
		Clock Timing							
Average clock period	tCK(avg)	0.625	100	0.535	100	0.468	100	ns	
Average High pulse width	tCH(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Average Low pulse width	tCL(avg)	0.46	0.54	0.46	0.54	0.46	0.54	tCK(avg)	
Absolute clock period	tCK(abs)	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) MIN + tJIT(per) MIN	-	tCK(avg) Min + tJIT(per) Min	-	ns	
Absolute High clock pulse width	tCH(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Absolute Low clock pulse width	tCL(abs)	0.43	0.57	0.43	0.57	0.43	0.57	tCK(avg)	
Clock period jitter	tJIT(per)	-40	40	-34	34	-30	30	ps	
Maximum Clock Jitter between consecutive cycles	tJIT(cc)	-	80	-	68	-	60	ps	

Table 53 – Core AC Timing

Parameter	Symbol	Min/ Max	Data Rate			Unit	Notes
Core Parameters			3200	3733	4266		
ACTIVATE-to-ACTIVATE command period (same bank)	tRC	MIN	tRAS + tRPab (with all bank precharge) tRAS + tRPpb (with per bank precharge)			ns	
Minimum Self Refresh Time (Entry to Exit)	tSR	MIN	max(15ns, 3nCK)			ns	
Self Refresh exit to next valid command delay	tXSR	MIN	max(tRFCab + 7.5ns, 2nCK)			ns	
Exit Power-Down to next valid command delay	tXP	MIN	max(7.5ns, 5nCK)			ns	
CAS-to-CAS delay	tCCD	MIN	8			tCK(avg)	
Internal READ to PRECHARGE command delay	tRTP	MIN	max(7.5ns, 8nCK)			ns	
RAS-to-CAS delay	tRCD	MIN	max(18ns, 4nCK)			ns	
Row precharge time (single bank)	tRPpb	MIN	max(18ns, 4nCK)			ns	
Row precharge time (all banks)	tRPab	MIN	max(21ns, 4nCK)			ns	
Row active time	tRAS	MIN	max(42ns, 3nCK)			ns	
		MAX	Min(9 * tREFI * Refresh Rate, 70.2) us (Refresh Rate is specified by MR4, OP[2:0])			-	
WRITE recovery time	tWR	MIN	max(18ns, 6nCK)			ns	
WRITE-to-READ delay	tWTR	MIN	max(10ns, 8nCK)			ns	
Active bank-A to active bank-B	tRRD	MIN	max(10ns, 4nCK)		max(7.5ns, 4nCK)	ns	2
Precharge to Precharge Delay	tPPD	MIN	4			tCK(avg)	1
Four-bank ACTIVATE window	tFAW	MIN	40		30	ns	2

Notes:
1. Precharge to precharge timing restriction does not apply to Auto-Precharge commands.

2. Devices supporting 4266 Mbps specification shall support these timings at lower data rates.
3. The value is based on BL16. For BL32 need additional 8 tCK(avg) delay.Table 54 – Read output timings (Unit UI = tCK(avg)min/2)

Parameter	Symbol	LPDDR4-3200		LPDDR4-3733		LPDDR4-4266		Units	Notes
		Min	Max	Min	Max	Min	Max		
Data Timing									
DQS_t,DQS_c to DQ Skew total, per group, per access (DBI-Disabled)	tDQSQ	-	0.18	-	0.18	-	0.18	UI	
DQ output hold time total from DQS_t, DQS_c (DBI-Disabled)	tQH	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	min(tQSH, tQSL)	-	UI	
DQ output window time total, per pin (DBI-Disabled)	tQW_total	0.7	-	0.7	-	0.7	-	UI	3
DQ output window time deterministic, per pin (DBI-Disabled)	tQW_dj	tbd	-	tbd	-	tbd	-	UI	2,3
DQS_t,DQS_c to DQ Skew total,per group, per access (DBI-Enabled)	tDQSQ_DBI	-	0.18	-	0.18	-	0.18	UI	
DQ output hold time total from DQS_t, DQS_c (DBI-Enabled)	tQH_DBI	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	min(tQSH_DBI, tQSL_DBI)	-	UI	
DQ output window time total, per pin (DBI-Enabled)	tQW_total_DBI	0.70	-	0.70	-	0.70	-	UI	3
Data Strobe Timing									
DQS, DQS# differential output low time (DBI-Disabled)	tQSL	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCL(abs) -0.05	-	tCK(avg)	3,4
DQS, DQS# differential output high time (DBI-Disabled)	tQSH	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCH(abs) -0.05	-	tCK(avg)	3,5
DQS, DQS# differential output low time (DBI-Enabled)	tQSL_DBI	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCL(abs) -0.045	-	tCK(avg)	4,6
DQS, DQS# differential output high time (DBI-Enabled)	tQSH_DBI	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCH(abs) -0.045	-	tCK(avg)	5,6

Notes:

1. The deterministic component of the total timing. Measurement method tbd.
2. This parameter will be characterized and guaranteed by design.
3. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.
4. tQSL describes the instantaneous differential output low pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
5. tQSH describes the instantaneous differential output high pulse width on DQS_t - DQS_c, as it measured the next rising edge from an arbitrary falling edge.
6. This parameter is function of input clock jitter. These values assume the min tCH(abs) and tCL(abs). When the input clock jitter min tCH(abs) and tCL(abs) is 0.44 or greater of tck(avg) the min value of tQSL will be tCL(abs)-0.04 and tQSH will be tCH(abs) -0.04.

Table 54 – Read AC Timing

Parameter	Symbol	Min/Max	Data Rate			Unit	Notes
Read Timing			3200	3733	4266		
READ preamble	tRPRE	Min	1.8			tCK(avg)	
0.5 tCK READ postamble	tRPST	Min	0.4			tCK(avg)	
1.5 tCK READ postamble	tRPST	Min	1.4			tCK(avg)	
DQ low-impedance time from CK_t, CK_c	tLZ(DQ)	Min	(RL x tCK) + tDQSCK(Min) - 200ps			ps	
DQ high impedance time from CK_t, CK_c	tHZ(DQ)	Max	(RL x tCK) + tDQSCK(Max) + tDQSQ(Max) + (BL/2 x tCK)-100ps			ps	
DQS_c low-impedance time from CK_t, CK_c	tLZ(DQS)	Min	(RL x tCK) + tDQSCK(Min) -(tRPRE(Max) x tCK) - 200ps			ps	
DQS_c high impedance time from CK_t, CK_c	tHZ(DQS)	Max	(RL x tCK) + tDQSCK(Max) +(BL/2 x tCK) + (RPST(Max) x tCK) - 100ps			ps	
DQS-DQ skew	tDQSQ	Max	0.18			UI	

Table 55 – tDQSCK Timing

Parameter	Symbol	Min	Max	Unit	Notes
DQS Output Access Time from CK_t/CK_c	tDQSCK	1.5	3.5	ns	1
DQS Output Access Time from CK_t/CK_c - Temperature Variation	tDQSCK_temp	-	4	ps/°C	2
DQS Output Access Time from CK_t/CK_c - Voltage Variation	tDQSCK_volt	-	7	ps/mV	3
CK to DQS Rank to Rank variation	tDQSCK_rank2rank	-	1.0	ns	4,5

Notes:

1. Includes DRAM process, voltage and temperature variation. It includes the AC noise impact for frequencies> 20 MHz and max voltage of 45 mV pk-pk from DC-20 MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC Operating conditions.
2. tDQSCK_temp max delay variation as a function of Temperature.
3. tDQSCK_volt max delay variation as a function of DC voltage variation for V_{DDQ} and V_{DD2}. tDQSCK_volt should be used to calculate timing variation due to V_{DDQ} and V_{DD2} noise < 20 MHz. Host controller do not need to account for any variation due to V_{DDQ} and V_{DD2} noise > 20 MHz. The voltage supply noise must comply to the component Min-Max DC Operating conditions. The voltage variation is defined as the Max[abs{tDQSCKmin@V1- tDQSCKmax@V2}, abs{tDQSCKmax@V1-tDQSCKmin@V2}]/abs{V1-V2}. For tester measurement V_{DDQ} = V_{DD2} is assumed.
4. The same voltage and temperature are applied to tDQS2CK_rank2rank.
5. tDQSCK_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

Table 56 – DRAM DQs In Receive Mode (UI = tCK(avg)min/2)

Symbol	Parameter	3200		3733		4266		Unit	Notes
		min	max	min	max	min	max		
VdIVW_total	Rx Mask voltage - p-p total	-	140	-	140	-	120	mV	1,2,3,4
TdIVW_total	Rx timing window total (At VdIVW voltage levels)	-	0.25	-	0.25	-	0.25	UI	1.2,4
TdIVW_1bit	Rx timing window 1 bit toggle (At VdIVW voltage levels)	-	TBD	-	TBD	-	TBD	UI	1,2,4, 12
VIHL_AC	DQ AC input pulse amplitude pk-pk	180	-	180	-	170	-	mV	5,13
TdIPW DQ	Input pulse width (At Vcent_DQ)	0.45		0.45		0.45		UI	6
tDQS2DQ	DQ to DQS offset	200	800	200	800	200	800	ps	7
tDQ2DQ	DQ to DQ offset	-	30	-	30	-	30	ps	8
tDQS2DQ_temp	DQ to DQS offset temperature variation	-	0.6	-	0.6	-	0.6	ps/°C	9
tDQS2DQ_volt	DQ to DQS offset voltage variation	-	33	-	33	-	33	ps/50 mV	10
SRIN_dIVW	Input Slew Rate over VdIVWJotal	1	7	1	7	1	7	V/ns	11
tDQS2DQ_rank2rank	DQ to DQS offset rank to rank variation	-	200	-	200	-	200	ps	14,15

Notes:

1. Data Rx mask voltage and timing parameters are applied per pin and includes the DRAM DQ to DQS voltage AC noise impact for frequencies >20 MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. The voltage supply noise must comply to the component Min-Max DC operating conditions.
2. The design specification is a BER <TBD. The BER will be characterized and extrapolated if necessary using a dual dirac method.
3. Rx mask voltage VdIVW total(max) must be centered around Vcent_DQ(pin_mid).
4. Vcent_DQ must be within the adjustment range of the DQ internal Vref.
5. DQ only input pulse amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_DQ(pin_mid) such that VIHL_AC/2 min must be met both above and below Vcent_DQ.
6. DQ only minimum input pulse width defined at the Vcent_DQ(pin_mid).
7. DQ to DQS offset is within byte from DRAM pin to DRAM internal latch. Includes all DRAM process, voltage and temperature variation.
8. DQ to DQ offset defined within byte from DRAM pin to DRAM internal latch for a given component.
9. TDQS2DQ max delay variation as a function of temperature.
10. TDQS2DQ max delay variation as a function of the DC voltage variation for V_{DDQ} and V_{DD2}. It includes the V_{DDQ} and V_{DD2} AC noise impact for frequencies > 20MHz and max voltage of 45mv pk-pk from DC-20MHz at a fixed temperature on the package. For tester measurement V_{DDQ} = V_{DD2} is assumed.
11. Input slew rate over VdIVW Mask centered at Vcent_DQ(pin_mid).
12. Rx mask defined for a one pin toggling with other DQ signals in a steady state.
13. VIHL_AC does not have to be met when no transitions are occurring.
14. The same voltage and temperature are applied to tDQS2DQ_rank2rank.
15. tDQS2DQ_rank2rank parameter is applied to multi-ranks per byte lane within a package consisting of the same design dies.

Table 57 – Write AC Timing

Parameter	Symbol	Min/Max	Data Rate			Unit	Notes
Write Timing			3200	3733	4266		
Write command to 1st DQS latching	tDQSS	Min	0.75			tCK(avg)	
		Max	1.25				
DQS input high-level	tDQSH	Min	0.4			tCK(avg)	
DQS input low-level width	tDQSL	Min	0.4			tCK(avg)	
DQS falling edge to CK setup time	tDSS	Min	0.2			tCK(avg)	
DQS falling edge hold time from CK	tDSH	Min	0.2			tCK(avg)	
Write preamble	tWPRE	Min	1.8			tCK(avg)	
0.5 tCK Write postamble	tWPST	Min	0.4			tCK(avg)	1
1.5 tCK Write postamble	tWPST	Min	1.4			tCK(avg)	1

Note 1: The length of Write Postamble depends on MR3 OP1 setting.

Table 58 – Power-Down AC Timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Notes
Power Down Timing					
CKE minimum pulse width (HIGH and LOW pulse width)	tCKE	Min	Max(7.5ns, 4nCK)	-	
Delay from valid command to CKE input LOW	tCMDCKE	Min	Max(1.75ns, 3nCK)	ns	1
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input Low	tCSCKE	Min	1.75	ns	
Valid CS Requirement after CKE Input low	tCKELCS	Min	Max(5ns, 5nCK)	ns	
Valid Clock Requirement before CKE Input High	tCKCKEH	Min	Max(1.75ns, 3nCK)	ns	1
Exit power- down to next valid command delay	tXP	Min	Max(7.5ns, 5nCK)	ns	1
Valid CS Requirement before CKE Input High	tCSCKEH	Min	1.75	ns	
Valid CS Requirement after CKE Input High	tCKEHCS	Min	Max(7.5ns, 5nCK)	ns	
Valid Clock and CS Requirement after CKE Input low after MRW Command	tMRWCKEL	Min	Max(14ns, 10nCK)	ns	1
Valid Clock and CS Requirement after CKE Input low after ZQ Calibration Start Command	tZQCKE	Min	Max(1.75ns, 3nCK)	ns	1

Note 1: Delay time has to satisfy both analog time(ns) and clock count(nCK).

Table 59 – Command Address Input Parameters (UI = tCK(avg)min)

Symbol	Parameter	DQ-3200		DQ-4266		Unit	Notes
		min	max	min	max		
VclVW	Rx Mask voltage - p-p	-	155	-	145	mV	1,2,3
TclVW	Rx timing window	-	0.3	-	0.3	UI	1,2,3
VIHL_AC	CA AC input pulse amplitude pk-pk	190	-	180	-	mV	4,7
TclPW	CA input pulse width	0.6		0.6		UI	5
SRIN_clVW	Input Slew Rate over VclVW	1	7	1	7	V/ns	6

Notes:
1. CA Rx mask voltage and timing parameters at the pin including voltage and temperature drift.
2. Rx mask voltage VclVW total(max) must be centered around Vcent_CA(pin mid).
3. Vcent_CA must be within the adjustment range of the CA internal Vref.
4. CA only input pulse signal amplitude into the receiver must meet or exceed VIHL AC at any point over the total UI. No timing requirement above level. VIHL AC is the peak to peak voltage centered around Vcent_CA(pin mid) such that VIHL_AC/2 min must be met both above and below Vcent_CA.
5. CA only minimum input pulse width defined at the Vcent_CA(pin mid).
6. Input slew rate over VclVW Mask centered at Vcent_CA(pin mid).
7. VIHL_AC does not have to be met when no transitions are occurring.

Table 60 – Mode Register Read/Write AC timing

Parameter	Symbol	Min/ Max	Data Rate	Unit	Notes
Mode Register Read/Write Timing					
Additional time after tXP has expired until MRR command may be issued	tMRRI	Min	tRCD + 3nCK	-	
MODE REGISTER READ command period	tMRR	Min	8	nCK	
MODE REGISTER WRITE command period	tMRW	Min	MAX(10ns, 10nCK)	-	
|Mode register set command delay	tMRD	Min	max(14ns, 10nCK)	-	

Table 61 – Asynchronous ODT Turn On and Turn Off Timing

Parameter	800-2133 MHz	Unit	Notes
tODTon, min	1.5	ns	
tODTon, max	3.5	ns	
tODToff, min	1.5	ns	
tODToff, max	3.5	ns	

Table 62 – Self-Refresh Timing Parameters

Parameter	Symbol	Min/Max	Data Rate	Unit	Note
Self Refresh Timing					
Delay from SRE command to CKE Input low	tESCKE	Min	Max(1.75ns, 3tCK)	ns	1
Minimum Self Refresh Time	tSR	Min	Max(15ns, 3tCK)	ns	1
Exit Self Refresh to Valid commands	tXSR	Min	Max(tRFCab + 7.5ns, 2tCK)	ns	1,2

Notes:
1. Delay time has to satisfy both analog time(ns) and clock count(tCK). It means that tESCKE will not expire until CK has toggled through at least 3 full cycles (3 *tCK) and 1.75ns has transpired.
2. MRR-1, CAS-2, DES, MPC, MRW-1 and MRW-2 except PASR Bank/Segment setting are only allowed during this period.

Table 63 – Command Bus Training AC Timing

Parameter	Symbol	Min/ Max	Data Rate			Unit	Notes
			3200	3733	4266		
Command Bus Training Timing							
Valid Clock Requirement after CKE Input low	tCKELCK	Min	Max(5ns, 5nCK)			-	
Data Setup for VREF Training Mode	tDStrain	Min	2			ns	
Data Hold for VREF Training Mode	tDHtrain	Min	2			ns	
Asynchronous Data Read	tADR	Max	20			ns	
CA Bus Training Command to CA Bus Training Command Delay	tCACD	Min	RU(tADR/tCK)			tCK	2
Valid Strobe Requirement before CKE Low	tDQSCKE	Min	10			ns	1
First CA Bus Training Command Following CKE Low	tCAENT	Min	250			ns	
VREF Step Time -multiple steps	tVREFCA_LONG	Max	250			ns	
Vref Step Time -one step	tVREFCA_SHORT	Max	80			ns	
Valid Clock Requirement before CS High	tCKPRECS	Min	2tck + tXP (tXP = max(7.5ns, 5nCK))			-	
Valid Clock Requirement after CS High	tCKPSTCS	Min	max(7.5ns, 5nCK))			-	
Minimum delay from CS to DQS toggle in command bus training	tCS_VREF	Min	2			tCK	
Minimum delay from CKE High to Strobe High Impedance	tCKEHDQS		10			ns	
Valid Clock Requirement before CKE input High	tCKCKEH	Min	Max(1.75ns, 3nCK)			-	
CA Bus Training CKE High to DQ Tri-state	tMRZ	Min	1.5			ns	
ODT turn-on Latency from CKE	tCKELODTon	Min	20			ns	
ODT tum-off Latency from CKE	tCKELODToff	Min	20			ns	
Exit Command Bus Training Mode to next valid command delay	tXCBT_Short	Min	Max(5nCK, 200ns)			-	3
	tXCBT_Middle	Min	Max(5nCK, 200ns)			-	
	tXCBT_Long	Min	Max(5nCK, 250ns)			-	

Notes:

1. DQS_t has to retain a low level during tDQSCKE period, as well as DQS_c has to retain a high level.
2. If tCACD is violated, the data for samples which violate tCACD will not be available, except for the last sample (where tCACD after this sample is met). Valid data for the last sample will be available after tADR.
3. Exit Command Bus Training Mode to next valid command delay Time depends on value of VREF(CA) setting: MR12 OP[5:0] and VREF(CA) Range: MR12 OP[6] of FSP-OP 0 and 1. Additionally exit Command Bus Training Mode to next valid command delay Time may affect VREF(DQ) setting. Settling time of VREF(DQ) level is same as VREF(CA) level.

Table 64 – Temperature Derating AC Timing

Parameter	Symbol	Min/ Max	Data Rate			Unit	Note
			3200	3733	4266		
Temperature Derating							1
DQS output access time from CK_t/CK_c (derated)	tDQSCK	MAX	3600			ps	
RAS-to-CAS delay (derated)	tRCD	MIN	tRCD+ 1.875			ns	
ACTIVATE-to- ACTIVATE command period (derated)	tRC	MIN	tRC + 3.75			ns	
Row active time (derated)	tRAS	MIN	tRAS + 1.875			ns	
Row precharge time (derated)	tRP	MIN	tRP+ 1.875			ns	
Active bank A to active bank B (derated)	tRRD	MIN	tRRD + 1.875			ns	

Note 1: Timing derating applies for operation at 85 °C to 105 °C.

3.3 IDD Specification

V_{DD2}, V_{DDQ} = 1.06 ~ 1.17V, V_{DD1} = 1.70 ~ 1.95V

Table 65 – LPDDR4 IDD Specification (4266Mbps)

Parameter	Supply	4Gb x16		8Gb x32		
		105℃	95℃	105℃	95℃	Unit
IDD01	V_{DD1}	22	15	49	31	mA
IDD02	V_{DD2}	58	50	115	101	mA
IDD0Q	V_{DDQ}	0.4	0.3	0.8	0.5	mA
IDD2P1	V_{DD1}	1.0	0.8	1.3	0.9	mA
IDD2P2	V_{DD2}	8.7	3.3	5.9	4.0	mA
IDD2PQ	V_{DDQ}	0.3	0.2	0.5	0.4	mA
IDD2PS1	V_{DD1}	1.0	0.8	1.3	1.0	mA
IDD2PS2	V_{DD2}	8.7	3.3	5.9	4.0	mA
IDD2PSQ	V_{DDQ}	0.3	0.3	0.5	0.4	mA
IDD2N1	V_{DD1}	14	4	29	11	mA
IDD2N2	V_{DD2}	33	27	57	54	mA
IDD2NQ	V_{DDQ}	0.3	0.3	0.5	0.4	mA
IDD2NS1	V_{DD1}	14	4	29	11	mA
IDD2NS2	V_{DD2}	16	10	22	19	mA
IDD2NSQ	V_{DDQ}	0.3	0.3	0.5	0.4	mA
IDD3P1	V_{DD1}	15	5	31	13	mA
IDD3P2	V_{DD2}	16	10	28	19	mA
IDD3PQ	V_{DDQ}	0.3	0.2	0.5	0.3	mA
IDD3PS1	V_{DD1}	15	5	31	13	mA
IDD3PS2	V_{DD2}	16	10	28	19	mA
IDD3PSQ	V_{DDQ}	0.3	0.2	0.5	0.3	mA
IDD3N1	V_{DD1}	15	5	31	13	mA
IDD3N2	V_{DD2}	41	34	78	69	mA
IDD3NQ	V_{DDQ}	0.4	0.4	0.8	0.6	mA
IDD3NS1	V_{DD1}	15	5	31	13	mA
IDD3NS2	V_{DD2}	24	17	42	34	mA
IDD3NSQ	V_{DDQ}	0.4	0.4	0.8	0.6	mA
IDD4R1	V_{DD1}	21	16	45	31	mA
IDD4R2	V_{DD2}	286	283	569	565	mA
IDD4RQ	V_{DDQ}	119	120	229	238	mA
IDD4W1	V_{DD1}	21	16	46	32	mA
IDD4W2	V_{DD2}	302	299	605	604	mA
IDD4WQ	V_{DDQ}	0.4	0.3	0.8	0.6	mA
IDD51	V_{DD1}	35	30	74	58	mA
IDD52	V_{DD2}	70	62	139	126	mA
IDD5Q	V_{DDQ}	0.4	0.3	0.7	0.5	mA
IDD5AB1	V_{DD1}	15	5	32	14	mA

Parameter	Supply	4Gb x16		8Gb x32		
		105℃	95℃	105℃	95℃	Unit
IDD5AB2	V_{DD2}	47	39	93	80	mA
IDD5ABQ	V_{DDQ}	0.3	0.3	0.5	0.4	mA
IDD5PB1	V_{DD1}	15	6	32	15	mA
IDD5PB2	V_{DD2}	48	40	94	81	mA
IDD5PBQ	V_{DDQ}	0.3	0.3	0.5	0.4	mA

V_{DD2}, V_{DDQ} = 1.06 ~ 1.17V, V_{DD1} = 1.70 ~ 1.95V

Table 66 – LPDDR4 IDD6 specification (4266Mbps)

Temperature	Parameter	Supply	4Gb x16	8Gb x32	Unit
25°C	IDD61	V_{DD1}	3	6	mA
	IDD62	V_{DD2}	6	5	mA
	IDD6Q	V_{DDQ}	0.2	0.8	mA
95°C	IDD61	V_{DD1}	3	6	mA
	IDD62	V_{DD2}	6	9	mA
	IDD6Q	V_{DDQ}	0.2	0.3	mA
105°C	IDD61	V_{DD1}	8	7	mA
	IDD62	V_{DD2}	11	12	mA
	IDD6Q	V_{DDQ}	0.2	0.5	mA

Notes:
1. IDD6 25°C is the typical, IDD6 95°C and IDD6 105°C are the maximum of the distribution of the arithmetic mean.
2. When T_C > 105°C, self-refresh mode is not available.

V_{DDQ} =0.57~0.65V, V_{DD2} = 1.06 ~ 1.17V, V_{DD1} = 1.70 ~ 1.95V

Table 67 – LPDDR4X IDD Specification (4266Mbps)

Parameter	Supply	4Gb x16		8Gb x32		
		105℃	95℃	105℃	95℃	Unit
IDD01	V_{DD1}	14	13	26	23	mA
IDD02	V_{DD2}	47	43	98	88	mA
IDD0Q	V_{DDQ}	0.2	0.2	0.3	0.3	mA
IDD2P1	V_{DD1}	0.5	0.4	1.2	0.9	mA
IDD2P2	V_{DD2}	1.9	1.3	7.1	2.6	mA
IDD2PQ	V_{DDQ}	0.1	0.1	0.2	0.2	mA
IDD2PS1	V_{DD1}	0.5	0.4	1.2	0.9	mA
IDD2PS2	V_{DD2}	1.9	1.3	7.1	2.6	mA
IDD2PSQ	V_{DDQ}	0.1	0.1	0.2	0.2	mA
IDD2N1	V_{DD1}	2.5	1.6	6.8	3.2	mA
IDD2N2	V_{DD2}	26	25	54	50	mA
IDD2NQ	V_{DDQ}	0.1	0.1	0.2	0.2	mA
IDD2NS1	V_{DD1}	2.5	1.6	6.7	3.2	mA
IDD2NS2	V_{DD2}	8.4	7.7	21	17	mA

Parameter	Supply	4Gb x16		8Gb x32		
		105℃	95℃	105℃	95℃	Unit
IDD2NSQ	V_{DDQ}	0.1	0.1	0.2	0.2	mA
IDD3P1	V_{DD1}	3.4	2.3	8.3	4.3	mA
IDD3P2	V_{DD2}	7.3	4.9	18	12	mA
IDD3PQ	V_{DDQ}	0.1	0.1	0.2	0.2	mA
IDD3PS1	V_{DD1}	3.4	2.2	8.3	4.3	mA
IDD3PS2	V_{DD2}	7.3	4.8	18	12	mA
IDD3PSQ	V_{DDQ}	0.1	0.1	0.2	0.2	mA
IDD3N1	V_{DD1}	3.4	2.3	8.3	4.3	mA
IDD3N2	V_{DD2}	32	30	66	60	mA
IDD3NQ	V_{DDQ}	0.2	0.2	0.4	0.3	mA
IDD3NS1	V_{DD1}	3.4	2.3	8.3	4.3	mA
IDD3NS2	V_{DD2}	15	13	32	26	mA
IDD3NSQ	V_{DDQ}	0.2	0.2	0.4	0.3	mA
IDD4R1	V_{DD1}	14	14	25	23	mA
IDD4R2	V_{DD2}	361	357	714	707	mA
IDD4RQ	V_{DDQ}	92	92	185	184	mA
IDD4W1	V_{DD1}	15	14	26	24	mA
IDD4W2	V_{DD2}	316	312	620	616	mA
IDD4WQ	V_{DDQ}	0.3	0.3	0.5	0.4	mA
IDD51	V_{DD1}	29	27	53	49	mA
IDD52	V_{DD2}	59	56	121	111	mA
IDD5Q	V_{DDQ}	0.2	0.2	0.3	0.2	mA
IDD5AB1	V_{DD1}	3.9	3.1	8.2	5.7	mA
IDD5AB2	V_{DD2}	35	32	76	65	mA
IDD5ABQ	V_{DDQ}	0.2	0.1	0.2	0.2	mA
IDD5PB1	V_{DD1}	4.5	3.7	9.0	6.7	mA
IDD5PB2	V_{DD2}	36	32	77	67	mA
IDD5PBQ	V_{DDQ}	0.2	0.1	0.2	0.2	mA

V_{DDQ} =0.57~0.65V, V_{DD2} = 1.06 ~ 1.17V, V_{DD1} = 1.70 ~ 1.95V

Table 68 – LPDDR4X IDD6 specification (4266Mbps)

Temperature	Parameter	Supply	4Gb x16	8Gb x32	Unit
25°C	IDD61	V_{DD1}	3	5	mA
	IDD62	V_{DD2}	3	5	mA
	IDD6Q	V_{DDQ}	0.1	0.1	mA
95°C	IDD61	V_{DD1}	3	6	mA
	IDD62	V_{DD2}	4	7	mA
	IDD6Q	V_{DDQ}	0.1	0.1	mA
105°C	IDD61	V_{DD1}	4	10	mA
	IDD62	V_{DD2}	5	12	mA
	IDD6Q	V_{DDQ}	0.1	0.2	mA

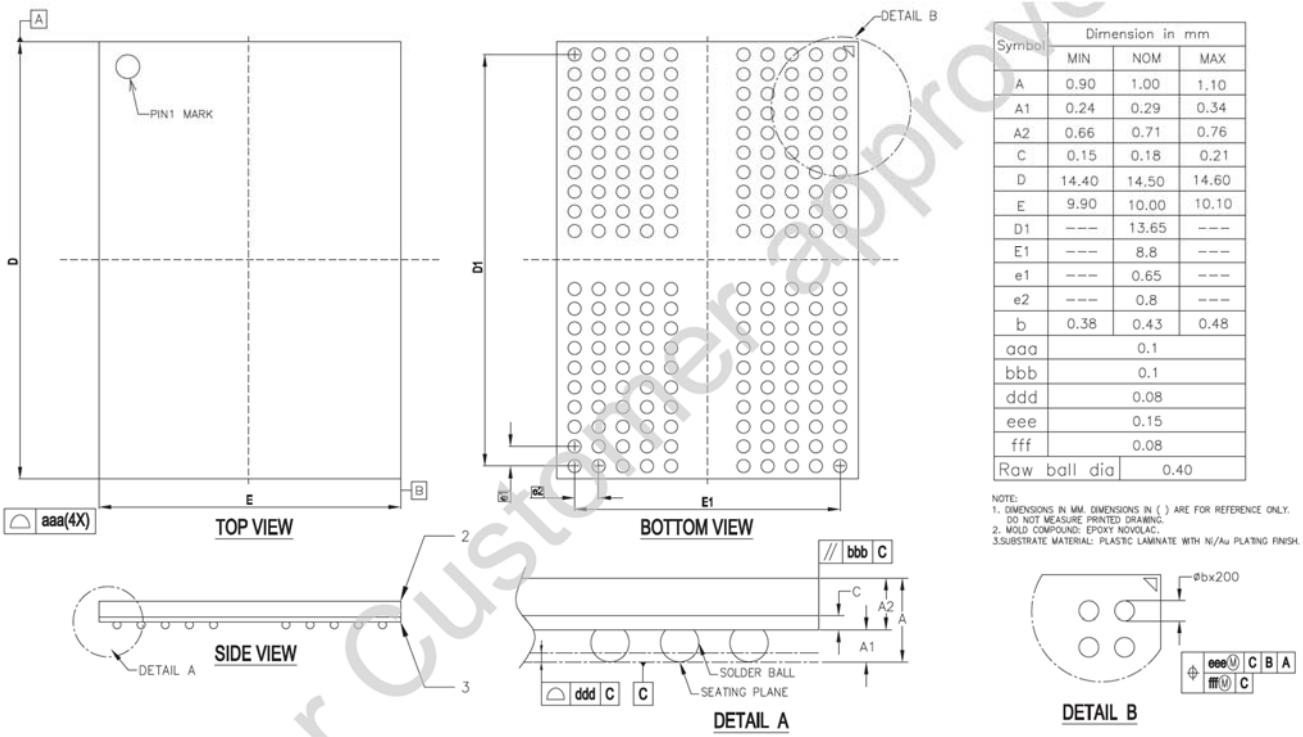
Notes:

1. IDD6 25°C is the typical, IDD6 95°C and IDD6 105°C are the maximum of the distribution of the arithmetic mean.
2. When T_C > 105°C, self-refresh mode is not available.

4 Package Outlines

Figure 26 reflects the current status of the outline dimensions of the LPDDR4/LPDDR4X SDRAM packages for components with x16/x32 configuration.

Figure 26 - Package Outline



Symbol	Dimension in mm		
	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.24	0.29	0.34
A2	0.66	0.71	0.76
C	0.15	0.18	0.21
D	14.40	14.50	14.60
E	9.90	10.00	10.10
D1	---	13.65	---
E1	---	8.8	---
e1	---	0.65	---
e2	---	0.8	---
b	0.38	0.43	0.48
aaa	0.1		
bbb	0.1		
ddd	0.08		
eee	0.15		
fff	0.08		
Raw ball dia	0.40		

NOTE:
1. DIMENSIONS IN MM. DIMENSIONS IN ( ) ARE FOR REFERENCE ONLY. DO NOT MEASURE PRINTED DRAWING.
2. MOLD COMPOUND: EPOXY NOVOLAC.
3.SUBSTRATE MATERIAL: PLASTIC LAMINATE WITH Ni/Au PLATING FINISH.

Package Material list and Process flow/Spec refer to “SCE11NxGxxxAF” product for automotive.

5 Product Type Nomenclature

For reference the UniIC SDRAM component nomenclature is enclosed in this chapter.

Table 69 – Examples for Nomenclature Fields

Example for	Field Number											
	1	2	3	4	5	6	7	8	9	10	11	12
LPDDR4 SDRAM	SC	B	11	N	4G	16	0	B	F	–	04Z	A2

Table 70 – Memory Nomenclature

Field	Description	Values	Coding
1	UniIC Component Prefix	SC	UniIC Identifier
2	Product Group	B	Commodity chip(no ECC)
3	Interface Voltage [V]	11	1.1V
4	DRAM Technology	N	LPDDR4
		R	LPDDR4X
5	Component Density [Gbit]	2G	2 Gbit
		4G	4 Gbit
		8G	8 Gbit
		16G	16 Gbit
6	Number of I/Os	40	× 4
		80	× 8
		16	×16
		32	x 32
7	Die Number	0	Mono die
		2	Dual die
8	Die Revision	A	First
		B	Second
		C	Third
9	Package, Lead-Free Status	C	FBGA, lead-containing
		F	FBGA, lead-free, 0.43 ball size
		H	
		I	
11	Power	–	Standard power product
		L	Low power product
	Speed Grade	06Y	LPDDR4-3200 28-28-28
		03A	LPDDR4-3733 32-32-32
		04Z	LPDDR4-4266 36-36-36
12	Temperature range	Blank	Commercial temperature range: 0 °C to 95 °C
		I	Industrial temperature range: -40 °C to 95 °C
		A1	Automotive temperature range, A1: -40 °C to 125 °C
		A2	Automotive temperature range, A2: -40 °C to 105 °C
		A25	Automotive temperature range, A25: -40 °C to 115 °C
		A3	Automotive temperature range, A3: -40 °C to 95 °C
		X	High-Rel temperature range: -55 °C to 125 °C

List of Figures

List of Tables

Edition 2025-07
Published by
Xi'an UniIC Semiconductors CO., Ltd.

Xi'an: 4th Floor, Building A,
No. 38 Gaoxin 6th Road,
Xian High-tech Industries Development Zone
Xi'an, Shaanxi 710075, P. R. China
Tel: +86-29-88318000
Fax: +86-29-88453299

info@unisemicon.com

Legal Disclaimer
THE INFORMATION GIVEN IN THIS INTERNET DATA SHEET SHALL IN NO EVENT BE REGARDED AS A GUARANTEE OF CONDITIONS OR CHARACTERISTICS. WITH RESPECT TO ANY EXAMPLES OR HINTS GIVEN HEREIN, ANY TYPICAL VALUES STATED HEREIN AND/OR ANY INFORMATION REGARDING THE APPLICATION OF THE DEVICE, UNIIC HEREBY DISCLAIMS ANY AND ALL WARRANTIES AND LIABILITIES OF ANY KIND, INCLUDING WITHOUT LIMITATION WARRANTIES OF NON-INFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS OF ANY THIRD PARTY.

Information
For further information on technology, delivery terms and conditions and prices please contact your nearest UniIC Office.

Warnings
Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest UniIC Office.
UniIC Components may only be used in life-support devices or systems with the express written approval of UniIC, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.
www.unisemicon.com