Dec. 2024

SCF1AW1C2A
SCF1AW2C2A
SCF1AW1I3A
SCF1AW2I3A

1Gb 1.8V SPI NAND

Data Sheet

Rev. B

Revision History		
Date	**Revision**	**Subjects (major changes since last revision)**
2024-11-14	A	Initial Release
2024-12-25	B	Update P/N

Contents

1. Features

- **Single-level cell (SLC) technology**
- **Organization**
  - Page size: 2112 bytes (2048 + 64)
  - Block size: 64 pages
  - Plane size: 1 plane with 1024 blocks
  - Device size: 1Gb with 1024 blocks
- **Serial Protocol Interface**
  - SPI clock polarity and phase Mode 0 and Mode 3
  - Standard SPI: SCK, CS#, SI, SO, WP#, Hold#
  - Dual SPI: SCK, CS#, SIO0, SIO1, WP#,Hold#
  - Quad SPI: SCK, CS#, SIO0, SIO1, SIO2, SIO3
- **Key Parameters**
  - Operation voltage

  · VCC: 1.7 To 1.95V
  - Operation temperature

  · Commercial: -20° C to +70° C

  · Industry: -40° C to +85° C
  - Clock frequency

  · 104MHz @1.8V (max)
  - Array Performance

  · Page Read: 22us (max) with on-die ECC disabled; 95us (max) with on- die ECC enabled

  · Page Program: 350us (typ) with on-die ECC disabled; 400us (typ) with on-die ECC enabled

  · Block Erase: 3ms (typ)

  · The internal ECC is designed as 8-bit/528bytes at least; when the internal ECC is disabled, the external 8-bit ECC is needed.
- **Advanced Command Set**
  - Read from Cache x2 (3Bh)
  - Read from Cache x4 (6Bh)
  - Program Load x4 (32h) / Program Load Random Data x4 (34h)
  - Permanent Block Lock Protection (2Ch)
- **Device Initialization**
  - Automatic device initialization with the First Page Data Auto Load on Power Up with ECC on always. To use this optional feature, user needs to write the first page with on-die ECC enabled.
- **Security**

  - Blocks 0-3 are valid when shipped from factory with ECC

  - Software Write Protection with Block Lock Register

  - Hardware Write Protection with WP# to freeze Block Protect (BP) bits

  - Lock Tight to freeze BP bits during one power cycle instead of WP#

  - Permanent Block Lock Protection

  OTP Space

  · 10 pages one-time programmable NAND Flash memory area
- **Quality and Reliability**
  - Data Retention: 10 years
  - Endurance: 60,000 P/E cycles for Commercial; 100,000 P/E cycles for Industry
- **Package**

  WSON8 (8mm x 6mm)

  WSON8 (5mm x 6mm)

2. Product list

Table shows all possible products within the 1Gb 1.8V NAND component generation.

Table 1 - Ordering Information for 1Gb 1.8V SPI NAND Components

Product Type	ECC	Endurance	speed	voltage	Package	Note
Commercial Temperature Range (-20°C to 70°C)						
SCF1AW1C2A	8bits	60K	104Mhz	1.8V	WSON8 6*8	
SCF1AW2C2A	8bits	60K	104Mhz	1.8V	WSON8 5*6	
Industrial Temperature Range (-40°C to 85°C)						
SCF1AW1I3A	8bits	100K	104Mhz	1.8V	WSON8 6*8	
SCF1AW2I3A	8bits	100K	104Mhz	1.8V	WSON8 5*6	

3. Packages and Pins

3.1 Package Type

SCF1AWXXXX is offered in WSON8 packages as shown in Figure 1. Package diagrams and dimensions are illustrated at the end of this datasheet.

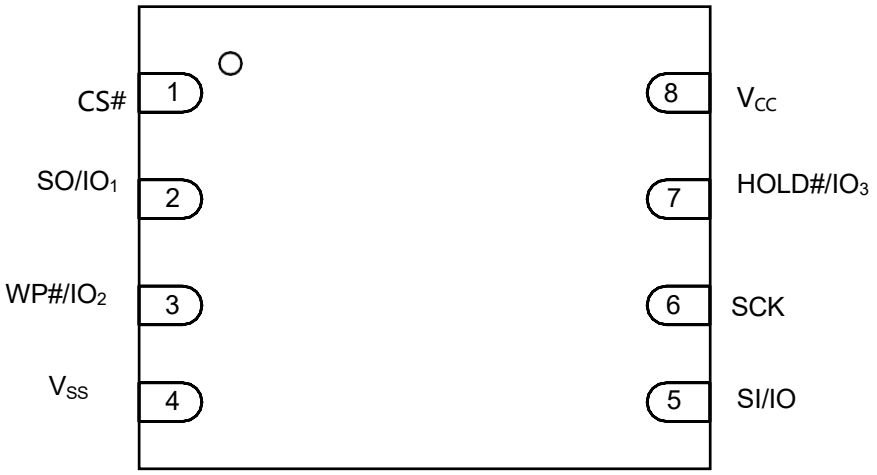


Figure 1: Pin Assignments of WSON8

3.2 Pin Description

Table 1: Pin Description

Symbol	Type	Name and function
CS#	Input	**Chip Select:** The device selection control.
SCK	Input	**Serial Clock:** The serial clock input.
SI/IO0	I/O	**Serial Data Input** or **Serial Data Input & Output** (for X2/X4 IO)**:** Transfer data serially into the device.
SO/IO1	I/O	**Serial Data Output** or **Serial Data Input & Output** (for X2/X4 IO)**:** Transfer data serially out of the device.
WP#/IO2	I/O	**Write Protect** or **Serial Data Input & Output** (for X4 IO)**:** Prevent the block lock bits from being overwritten.
HOLD#/IO3	I/O	**Hold** or **Serial Data Input & Output** (for X4 IO)**:** Pause any serial communication with the device without de-selecting it.
VCC	Supply	**Vcc:** The power supply for device.
VSS	Supply	**Vss:** Ground.

4. Block Diagram

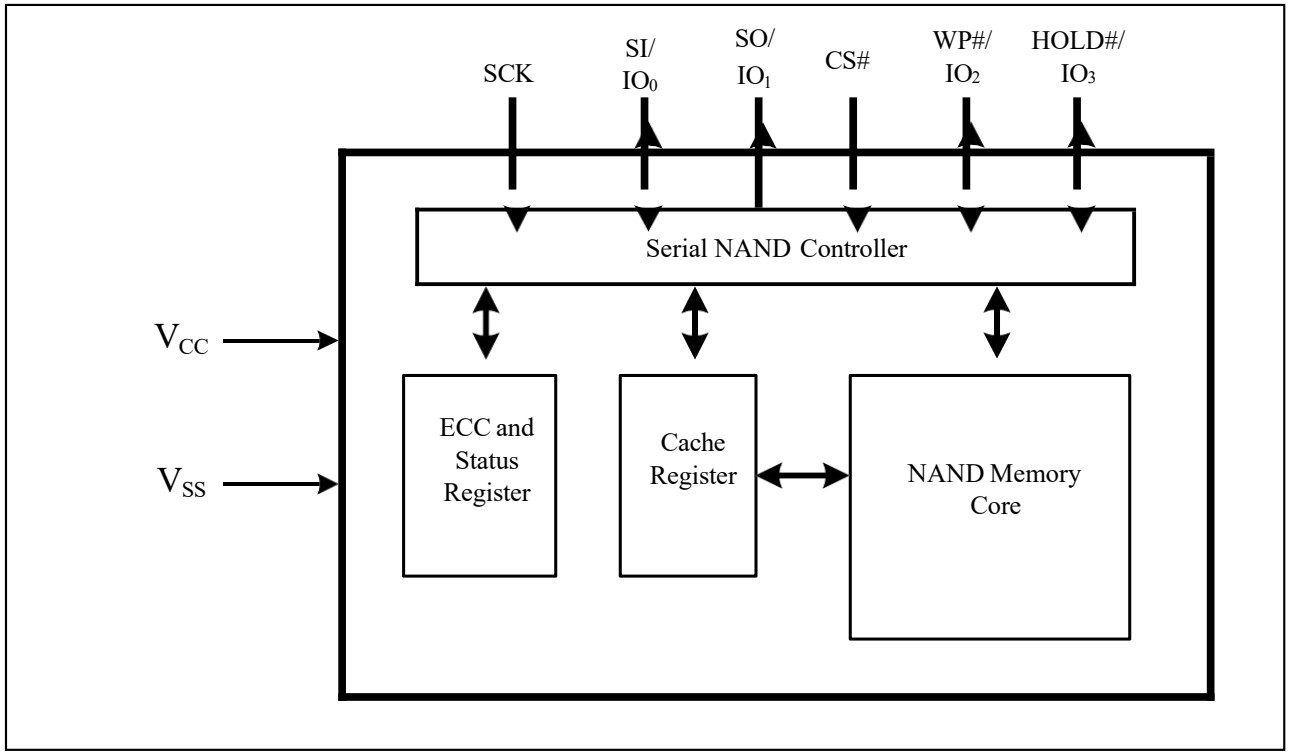


Figure 2: SPI NAND Flash Memory Block Diagram

5. Memory Mapping

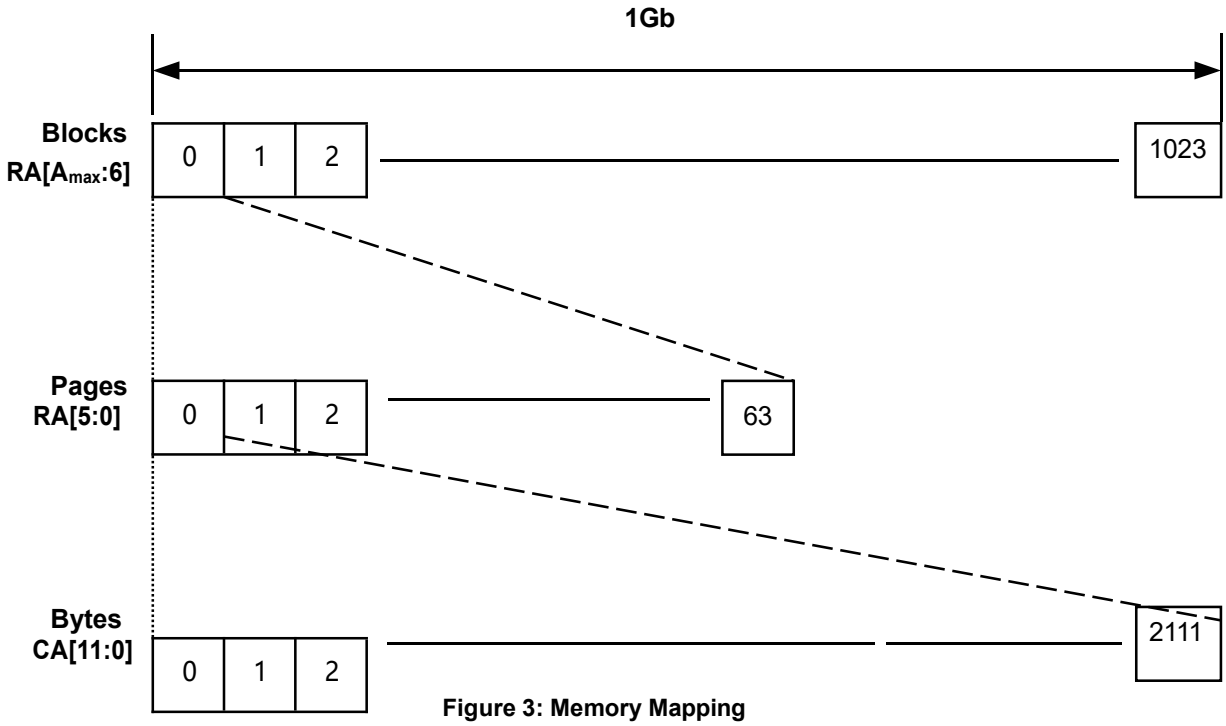


Figure 3: Memory Mapping

6. Array Organization

Array Organization:

- Page size: 2112 bytes (2048 + 64)
- Block size: 64 pages
- Plane size: 1 plane with 1024 blocks
- Device size: 1Gb with 1024 blocks

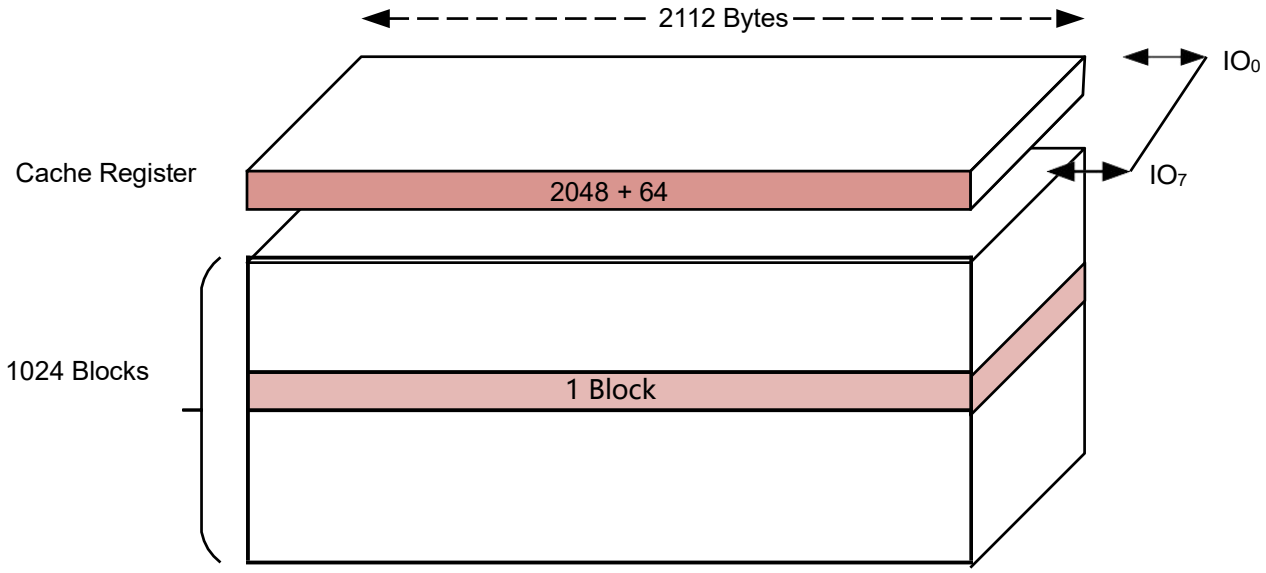


Figure 4: Array Organization

7. Device Operations

7.1 SPI Modes

SPI NAND supports two SPI modes:

- CPOL = 0, CPHA = 0 (Mode 0)
- CPOL = 1, CPHA = 1 (Mode 3)

Input data is latched in on the rising edge of SCK, and output data is available from the falling edge of SCK for both modes.

When the bus master is in standby mode:

- SCK remains at 0 for (CPOL = 0, CPHA = 0, Mode 0)
- SCK remains at 1 for (CPOL = 1, CPHA = 1, Mode 3)

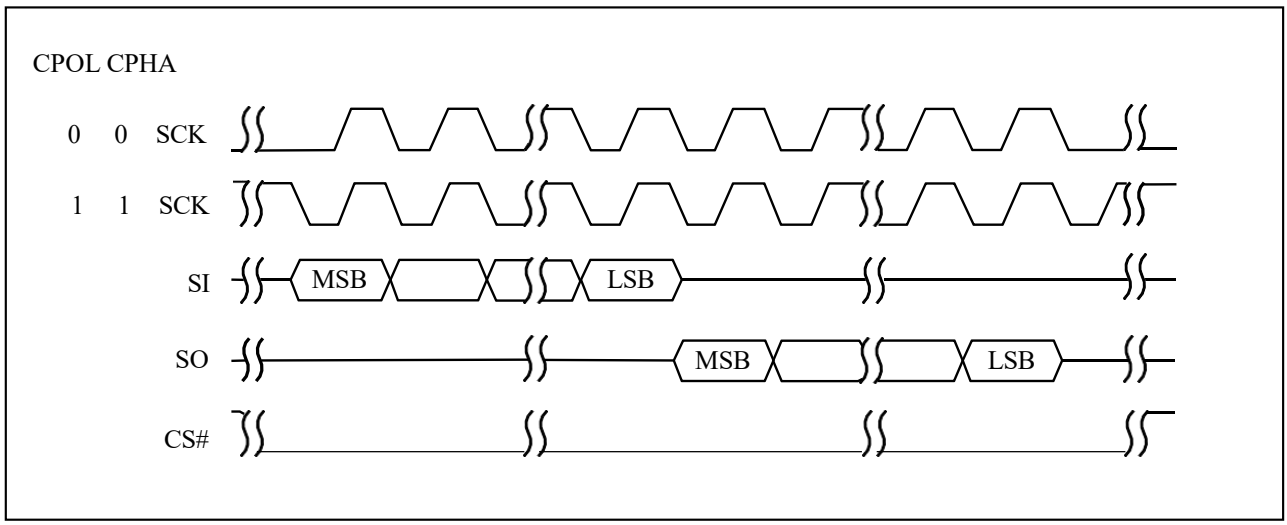


Figure 5: SPI Modes Timing

All timing diagrams shown in this datasheet are Mode 0.

7.2 SPI Protocols

The device supports two serial protocols:

- Standard SPI protocol
- Extended SPI protocol

Using different Command Op Codes can configure the device to one of these protocols.

7.2.1 Standard SPI

Instruction, addresses and data are transmitted on a single data line at standard SPI protocol. Instruction, address and Input data is latched in on the rising edge of SCK through SI; Output data is available from the falling edge of SCK through SO.

7.2.2 Extended SPI

An extension of the standard SPI protocol. Instructions and address are transmitted on a signal data line through SI, while data are transmitted by two or four data lines depending on the instruction.

7.3 Pin Descriptions

7.3.1 CS#

Chip select (CS#) activates or deactivates the device. When CS# goes LOW, the device is placed in active mode. When CS# is HIGH, the device is placed in inactive mode and IO is High-Z.

7.3.2 SCK

Serial clock (SCK) provides interface timing for SPI NAND. Commands, addresses, and data are latched on the rising edge of SCK. Data is placed on IO at the falling edge of SCK. When CS# is HIGH, SCK must return either HIGH or LOW.

7.3.3 SI/IO0

Writes use serial data in (SI). Commands, addresses, and data are transferred on SI in x1 mode at the rising edge of SCK. SI must not be driven by the host during x2 or x4 read operations.

IO_0 operation is enabled by issuing a READ FROM CACHE x2 or x4 command with data being clocked out of the device at the falling edge of SCK or by issuing a PROGRAM LOAD x4 or PROGRAM LOAD RANDOM DATA x4 with data being clocked into the device at the rising edge of SCK. During this time the host must wait until the READ FROM CACHE x2 or x4 command is complete before driving IO_0.

7.3.4 SO/IO1

Reads use serial data out (SO). Device reads are performed in x1, or x2, or x4 modes. SO acts as the only output in x1 READ operations, and as IO_1 in x2, x4 read operations or x4 write operation.

Data is clocked out of the device on SO/IO_1 at the falling edge of SCK control signals. When writing to the device in x4 mode, data is clocked into the device on SO/IO_1 at the rising edge of SCK control signals.

7.3.5 WP#/IO2

Write protect (WP#) prevents the block lock bits (BP0, BP1, BP2, INV and CMP) from being overwritten. If the BRWD bit is set to 1 and WP# is LOW, the block protect bits cannot be altered. WP# must not be driven by the host during READ FROM CACHE x4 operations.

IO_2 operation is enabled by issuing a READ FROM CACHE x4 command with data being clocked out of the device at the falling edge of SCK or by issuing a PROGRAM LOAD x4 or PROGRAM LOAD RANDOM DATA x4 with data being clocked into the device at the rising edge of SCK. During this time, the host must wait until the READ FROM CACHE x4 command is completed before driving WP#.

7.3.6 HOLD#/IO3

HOLD# input provides a method to pause serial communication with the device but does not terminate any ERASE, READ, or WRITE operation currently in progress.

Hold mode starts at the falling edge of HOLD# provided SCK is also LOW. If SCK is HIGH when HOLD# goes LOW, hold mode begins after the next falling edge of SCK. Similarly, hold mode is exited at the rising edge of HOLD# provided SCK is also LOW. If SCK is HIGH, hold mode ends after the next falling edge of SCK.

During hold mode, SO is High-Z, and SI and SCK inputs are ignored.

IO_3 operation is enabled by issuing a READ FROM CACHE x4 command with data being clocked out of the device at the falling edge of SCK or by issuing a PROGRAM LOAD x4 or PROGRAM LOAD RANDOM DATA x4 with data being clocked into the device at the rising edge of SCK. During this time, the host must wait until the READ FROM CACHE x4 command is completed before driving HOLD#.

8. Command Definition

8.1 Command Set Tables

Table 2: SPI NAND Command Set

Commands	Op Code	Address Bytes	Dummy Bytes	Data Bytes	Comments
RESET	FFh	0	0	0	Reset the device
GET FEATURE	0Fh	1	0	1	Get Features
SET FEATURE	1Fh	1	0	1	Set Features
PAGE READ	13h	3	0	0	Array Read
READ FROM CACHE	03h, 0Bh	2	1	1 to 2112	Output Cache data at Column address
READ FROM CACHE x2	3Bh	2	1	1 to 2112	Output Cache data on IO_0 and IO_1
READ FROM CACHE x4	6Bh	2	1	1 to 2112	Output Cache data on IO_0, IO_1, IO_2 and IO_3
BLOCK ERASE	D8h	3	0	0	Block Erase
PROGRAM EXECUTE	10h	3	0	0	Array Program
PROGRAM LOAD	02h	2	0	1 to 2112	Load Program data into Cache register
Program LOAD RANDOM DATA	84h	2	0	1 to 2112	Overwrite cache register with input data
PROGRAM LOAD x4	32h	2	0	1 to 2112	Load program data into cache register on IO_0, IO_1, IO_2 and IO_3
PROGRAM LOAD RANDOM DATA x4	34h	2	0	1 to 2112	Overwrite cache register with input data on IO_0, IO_1, IO_2 and IO_3
READ ID	9Fh	0	1	2	Read Device ID
WRITE DISABLE	04h	0	0	0	Set the WEL bit to 0
WRITE ENABLE	06h	0	0	0	Set the WEL bit to 1
PERMANENT BLOCK LOCK PROTECTION	2Ch	3	0	0	Provide nonvolatile and irreversible protection to boot blocks in groups.

In this product, every instruction sequence starts with one-byte instruction code. Depending on the instruction, the instruction sequence involves shifting in address bytes and/or data bytes. Some instructions do not have any address or data bytes.

In the case of Read (Get Feature, all types of read from cache, Read ID) instructions, the shifted-in instruction sequence is followed by a data-out sequence. Chip Select (CS#) can be driven high at any time during the data-out sequence.

In the case of write instructions (Block Erase, Program Execute, all types of Program Load, Write Enable, Write Disable, Permanent block Lock Protection, Set Feature), Page Read (13h) and Reset instructions, the Chip Select (CS#) must be driven high after whole instruction sequence is completed. Otherwise the instruction is not executed and the state of WEL remains unchanged if these instructions that alter the array or device configuration require Write Enable Latch (WEL) bit to be set.

8.2 Reset Operations

8.2.1 RESET (FFh)

The RESET command is used to put the memory device into a known condition and to abort the command sequence in progress.

Read, Program and Erase commands can be aborted while the device is in the busy state. The contents of the memory location being programmed or the block being erased are no longer valid. The data may be partially erased or programmed, and is invalid. The status register is cleared.

In SPI NAND protocol, RESET command also reset OTP_CFG2,1,0 (One Time Programmable Configuration Register Bits) back to normal operation. While all the other configuration register bits would not be reset by RESET command to keep the device configuration.

Once the RESET command is issued to the device, the device will take tRST to reset. During this period, no other command could be accepted except Get Feature command.

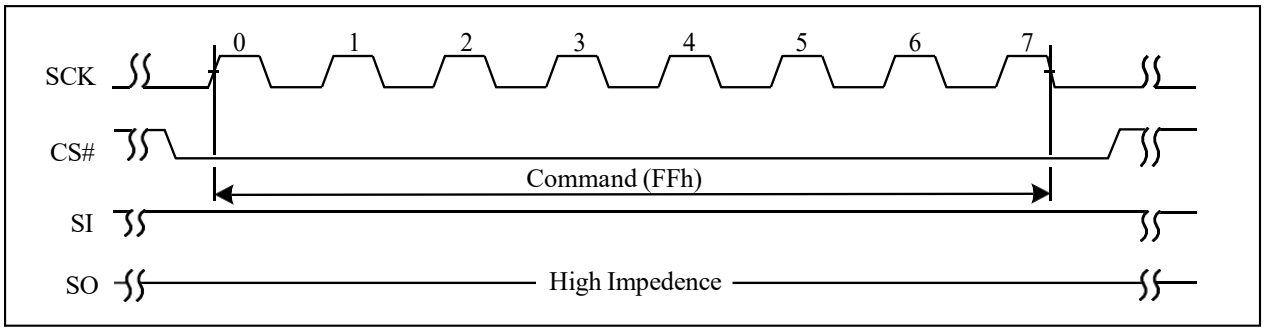


Figure 6: RESET (FFh) Timing

8.3 WRITE Operations

8.3.1 WRITE ENABLE (06h)

The WRITE ENABLE (06h) command sets the WEL bit in the status register to 1. WRITE ENABLE is required in the following operations that change the contents of the memory array:

- Page Program
- OTP Program
- Block Erase
- Permanent Block Lock Protection

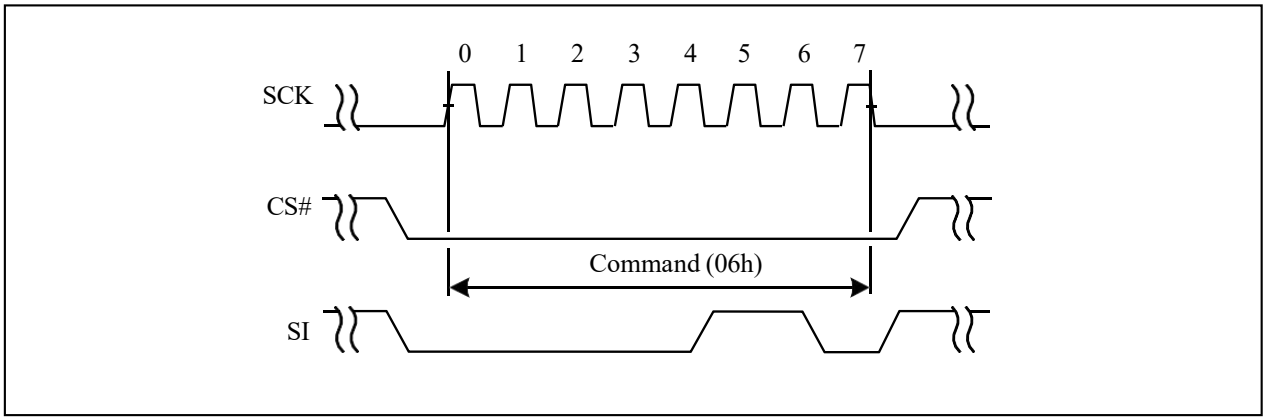


Figure 7: WRITE ENABLE (06h) Timing

8.3.2 WRITE DISABLE (04h)

The WRITE DISABLE (04h) command clears the WEL bit in the status register to 0. This disables the following operations:

- Page Program
- OTP Program
- Block Erase
- Permanent Block Lock Protection

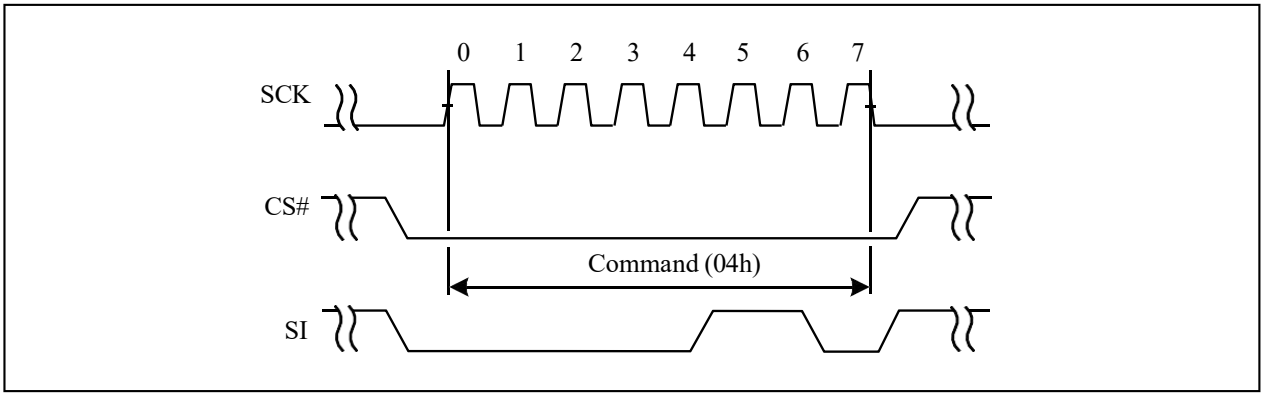


Figure 8: WRITE DISABLE (04h) Timing

8.4 Feature Operations

8.4.1 GET FEATURE (0Fh) and SET FEATURE (1Fh)

The GET FEATURE (0Fh) and SET FEATURE (1Fh) commands are used to alter the device behavior from the default power-on behavior. These commands use a 1-byte feature address to determine which feature is to be read or modified. Features such as OTP and block locking can be enabled or disabled by setting specific bits in feature address A0h and B0h. The status register is mostly read, except WEL, which is a writable bit with the WRITE ENABLE (06h) command.

When a feature is set, it remains active until the device is power cycled or the feature is written to by SET FEATURE command. Unless otherwise specified in the following table, once the device is set, it remains set, even if a RESET (FFh) command is issued.

Note: SET FEATURE command only could be executed during device ready state (OIP = 0); otherwise this command would be ignored.

Register	Address	Data Bits							
		7	6	5	4	3	2	1	0
Block Lock	A0h	BRWD[1]	Reserved	BP2	BP1	BP0	INV	CMP	Reserved
Configuration	B0h	OTP_CFG2	OTP_CFG1	LOT_Enable	ECC_Enable	Reserved	Reserved	OTP_CFG0	QE
Status	C0h	Reserved	ECCS2	ECCS1	ECCS0	P_FAIL	E_FAIL	WEL	OIP
Drive strength	D0h	Reserved	DRS1	DRS0	Reserved	Reserved	Reserved	Reserved	Reserved

Table 3: Feature Settings

Note:

1.If BRWD (block lock register write disabled) is enabled and WP# is LOW, then bits 7, 5, 4, 3, 2 and 1 at the Block Lock register cannot be changed

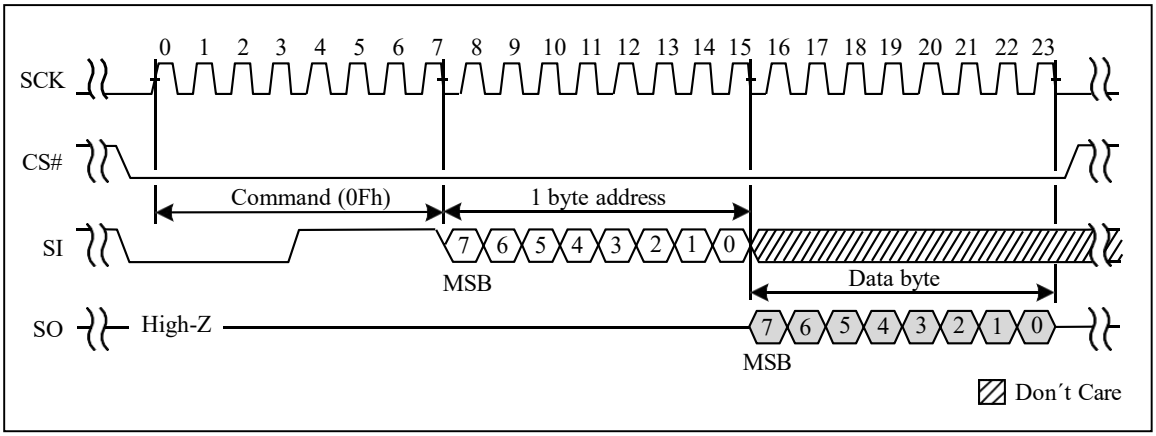


Figure 9: GET FEATURE (0Fh) Timing

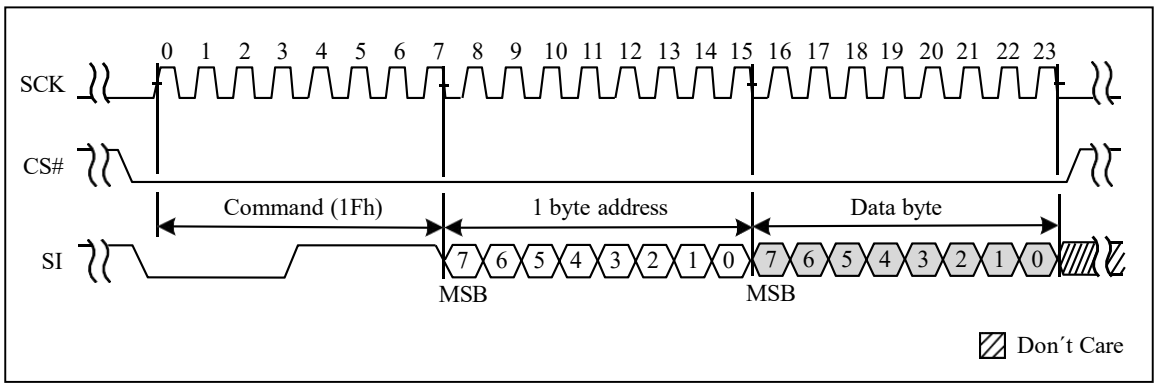


Figure 10: SET FEATURE (1Fh) Timing

8.4.2 Block Lock Register

This register contains volatile block protection bits and BRWD bit. The default value of this register is 3Eh after power up.

Bit	Name	Attribute	Description
7	BRWD	R/W	Default = 0; when BRWD = 1, enable hardware protection mode with WP# low
6	Reserved	Read Only	Default = 0
5	BP2	R/W	Default = 111XX to protect entire array
4	BP1	R/W	
3	BP0	R/W	
2	INV	R/W	
1	CMP	R/W	
0	Reserved	Read Only	Default = 0

Table 4: Block Lock Register

8.4.2.1 Volatile Block Protection

The volatile Block Protect bits (BP bits) (BP2, BP1, BP0), Invert bit (INV) and Complementary bit (CMP) in block lock register allow part of the memory or the entire array to be configured as read-only. The default value for the BP bits, INV and CMP bit are 1 after power up to protect the entire array.

The BP bits cannot be changed by SET FEATURE command when the BRWD bit is set to '1' and the WP# pin is driven low (Hardware protected mode). Noted when QE is set to '1', this hardware protected mode will be disabled.

8.4.2.2 BRWD bit (Block Lock Register Write Disable)

The BRWD bit is operated in conjunction with the Write protect (WP#) signal. The BRWD bit and WP# signal allow the device to be in the hardware protected mode (BRWD = 1 and WP# is low). In this mode, BP bits become read-only. The default value for BRWD bit is 0 after power up.

When QE is set to '1', hardware protected mode is disabled.

8.4.3 Configuration Register Bits

Table 5: Configuration Register Bits

Bit	Name	Attribute	Description
7	OTP_CFG2	R/W	Default = '000' to enable normal operation '010' to enable OTP access '110' to enable OTP data protection bit access '111' to enable Boot block lock protection configuration bit access others to enable normal operation
6	OTP_CFG1	R/W	
1	OTP_CFG0	R/W	
5	LOT_Enable	R/W	Default = 0 not to protect BP bits from changes
4	ECC_Enable	R/W	Default = 1 to indicate ECC on/off after device initialization
3	Reserved	Read Only	Default = 0
2	Reserved	Read Only	Default = 0
0	QE	R/W	Quad mode enable/disable bit; Default = 0 indicates Quad mode is disabled

8.4.3.1 OTP (One Time Programmable) Configuration Register Bits (OTP_CFG2,1,0)

In addition to the main memory array, a 10 pages OTP area of 2112-byte each is provided for the system to store critical data that cannot be changed once OTP DATA protection bit is set to '0'.

To protect boot block lock protection from further change, this product also provides a nonvolatile configuration to disable boot block lock protection for the user. This is also implemented through Program Execute by reserving one page of flash array to store this configuration bit.

OTP_CFG2,1,0 controls the access entry to above different operations. The default value after power up or a RESET command is 0.

8.4.3.2 Lock Tight Enable (LOT_ENABLE)

LOT_Enable bit provides a software protection to protect BP bits, INV and CMP bit when hardware protection mode is disabled for Quad operations.

Note that once this bit is set to '1', only power-down and power-up cycle could change this bit to '0' state.

8.4.3.3 ECC Enable (ECC_ENABLE)

This product has an on-die ECC algorithm that can be used to obtain the data integrity. Internal ECC calculation is done during page programming, and the result is stored in reserved ECC area for each page. During the array read operation, ECC engine will verify the data values according to stored ECC information and to make necessary corrections if needed. Correction status is indicated by the ECC status bits.

ECC_Enable = 1 indicates on-die ECC turned-on; conversely, ECC_Enable = 0 indicated on- die ECC turned-off.

ECC_Enable will be as "1" indicates on-die ECC turned on after device initialization. This bit could be changed by SET FEATURE command at feature address B0h; while RESET command could not change this bit to default value.

8.4.3.4 QE (Quad mode Enable bit)

QE bit is designed to support x4 mode and enable x4 mode commands. During x4 mode, WP#/HOLD# is used as IO_2/IO_3 respectively. The user might not drive these two pins during command or address cycles; this might cause some accidental hardware protection mode enabled or accidental HOLD condition entries in applications. This bit could be used to disable hardware protection mode and HOLD condition as well as enable x4 command acceptance.

8.4.4 Status Register

Status register bits shows the dice status; all bits are read-only register except WEL which could be changed by WRITE DISABLE (04h) and WRITE ENABE (06h) commands. None of bits could be changed by SET FEATURE (1Fh) command.

8.4.5 Drive Strength (DRS1, DRS0)

Output Drive Strength bits can be used to adjust output pin strength. Default Drive Strength bits (DRS1, DRS0) is (1, 0) which means default Drive Strength is 50%.

Table 6: Drive Strength Bits

DRS1	DRS0	Drive Strength
0	0	100%
0	1	75%
1	0	50%
1	1	25%

8.5 READ Operations

8.5.1 PAGE READ (13h)

The PAGE READ (13h) command transfers the data from the NAND Flash array to the cache register. The command sequence to transfer data from array to output is as follows:

- 13h (PAGE READ to cache register)
- 0Fh (GET FEATURE command to read the status)
- 03h or 0Bh (Read from Cache x1); or 3Bh (Read From Cache x2); or 6Bh (Read from Cache x4)

The PAGE READ command requires a 24-bit address consisting of 8 dummy bits followed by a 16-bit block/page address. After the block/page addresses are registered, the device starts the transfer from the main array to the cache register, and is busy for tRD time. During this time, the GET FEATURE (0Fh) command can be issued to monitor the status of the operation. Following a status of successful completion, the READ FROM CACHE command must be issued in order to read the data out of the cache. The READ FROM CACHE command requires 4 dummy bits, followed by a 12-bit column address for the

Starting byte address. The starting byte address can be 0 to 2111, but after the end of the cache register is reached, the data does not wrap around and SO goes to a High-Z state.

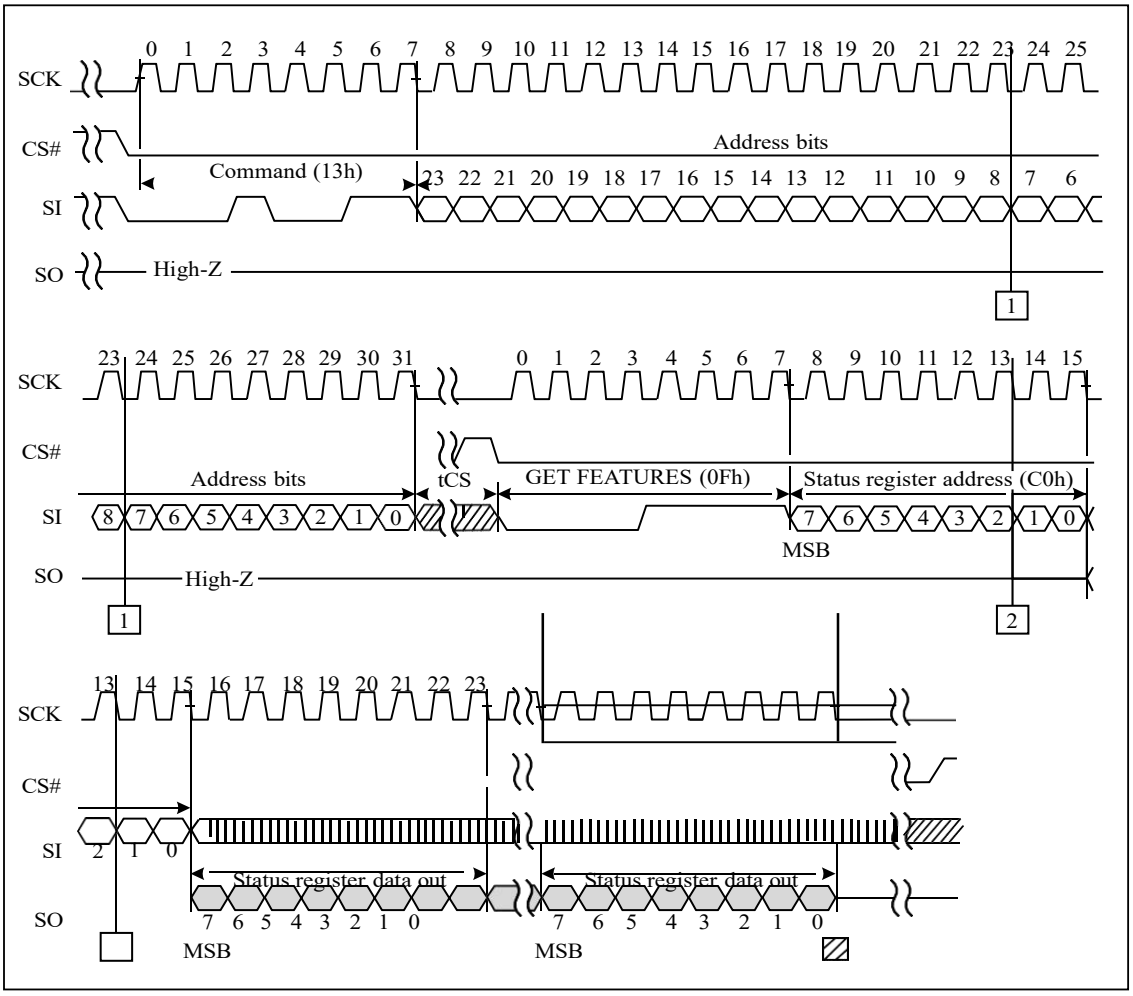


Figure 11: PAGE READ (13h) Timing

8.5.2 READ FROM CACHE x1 (03h or 0Bh)

The READ FROM CACHE x1 command allows one or more data bytes to be sequentially read from the cache buffer after executing this command. This command is initiated by driving the CS# pin low and then shifting the command op code (03h/0Bh) followed by the 16 bit column address and 8-bit dummy clocks. After the address is received, the data byte of the addressed cache buffer location will be shifted out on the SO pin at the falling edge of SCK with most significant bit (MSB) first. The address is automatically incremented to the next higher address after each byte of data is shifted out allowing for a continuous stream of data. This command is completed by driving CS# high.

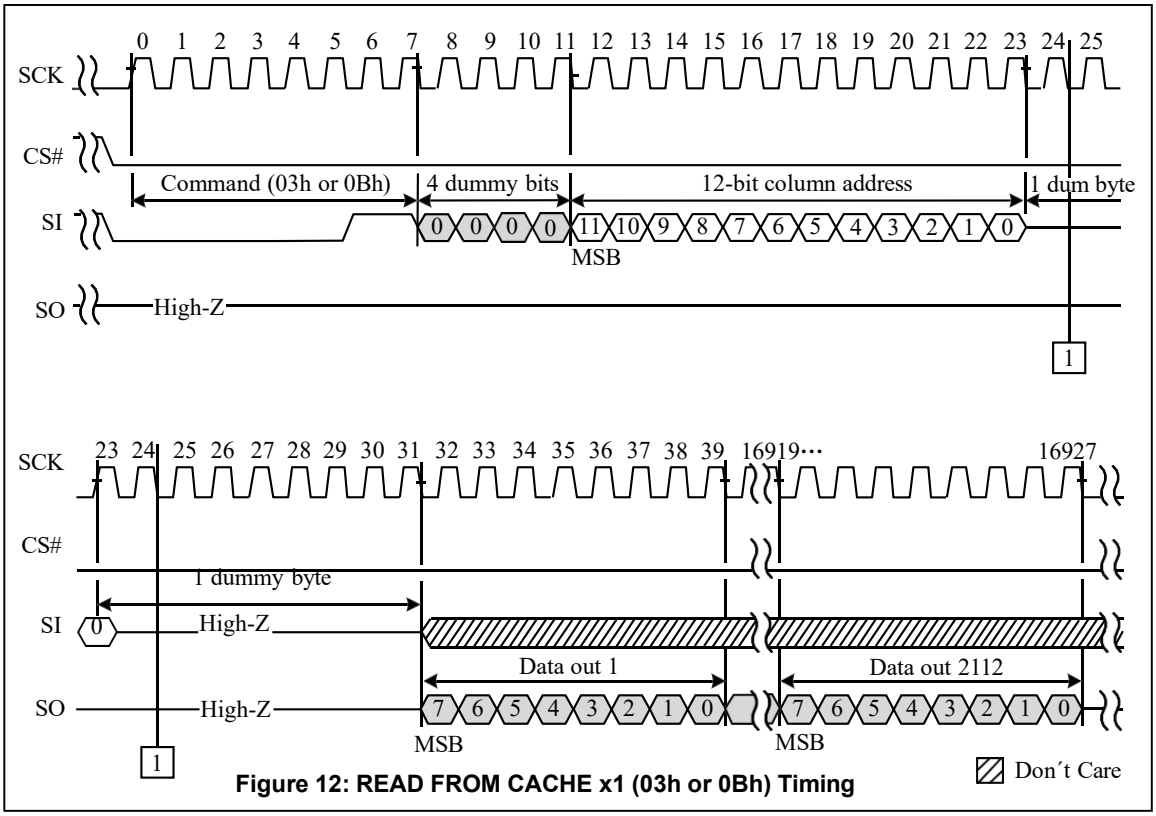


Figure 12: READ FROM CACHE x1 (03h or 0Bh) Timing

8.5.3 READ FROM CACHE x2 (3Bh)

The READ FROM CACHE x2 (3Bh) command is similar to Read from Cache (03h or 0Bh) except that data is output on two pins: IO_0 (SI) and IO_1 (SO). This allows data to be transferred at twice the rate of 03h/0Bh command.

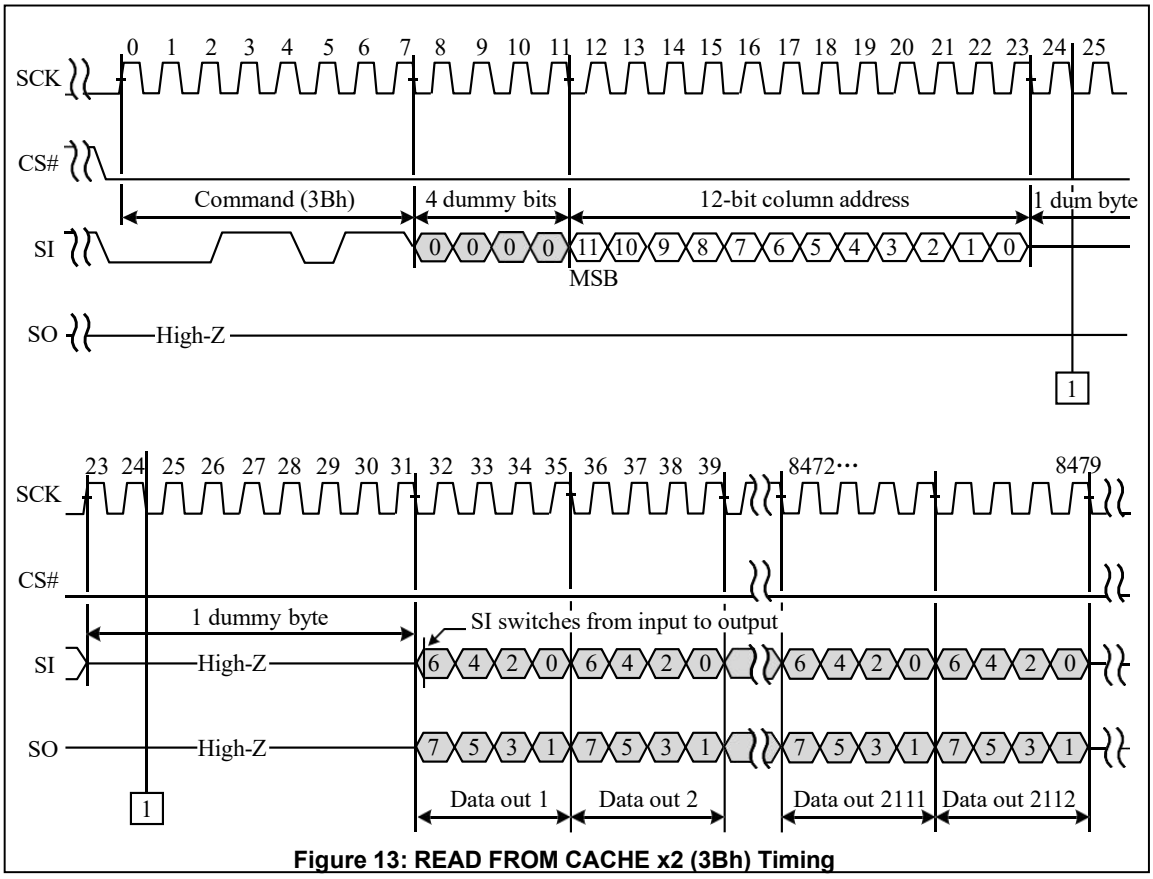


Figure 13: READ FROM CACHE x2 (3Bh) Timing

8.5.4 READ FROM CACHE x4 (6Bh)

The READ FROM CACHE x4 (6Bh) command is similar to Read from Cache (03h or 0Bh) except that data is output on four pins: IO_0, IO_1, IO_2 and IO_3. This allows data to be transferred at four times the rate of 03h/0Bh command.

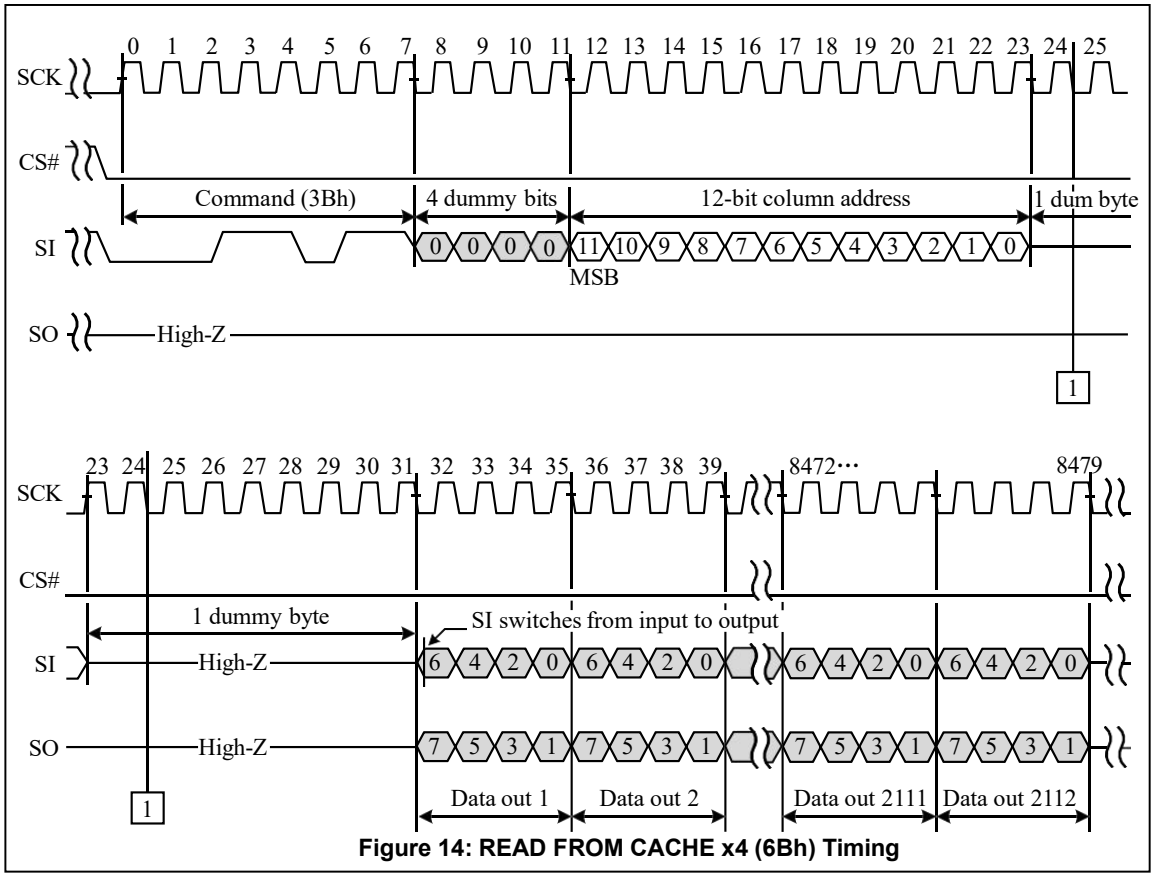


Figure 14: READ FROM CACHE x4 (6Bh) Timing

8.5.5 READ ID (9Fh)

The READ ID command is used to read the 2 bytes of identifier code programmed into the NAND Flash device. The READ ID command reads a 2-byte table (see below) that includes the Manufacturer ID and the device configuration.

Table 7: READ ID Table

Byte	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	Value
0	Manufacture ID (t.b.d)	0	0	0	1	1	0	1	0	1Ah
1	Device ID (1Gb, 1.8V)	0	0	0	1	0	1	0	1	15h

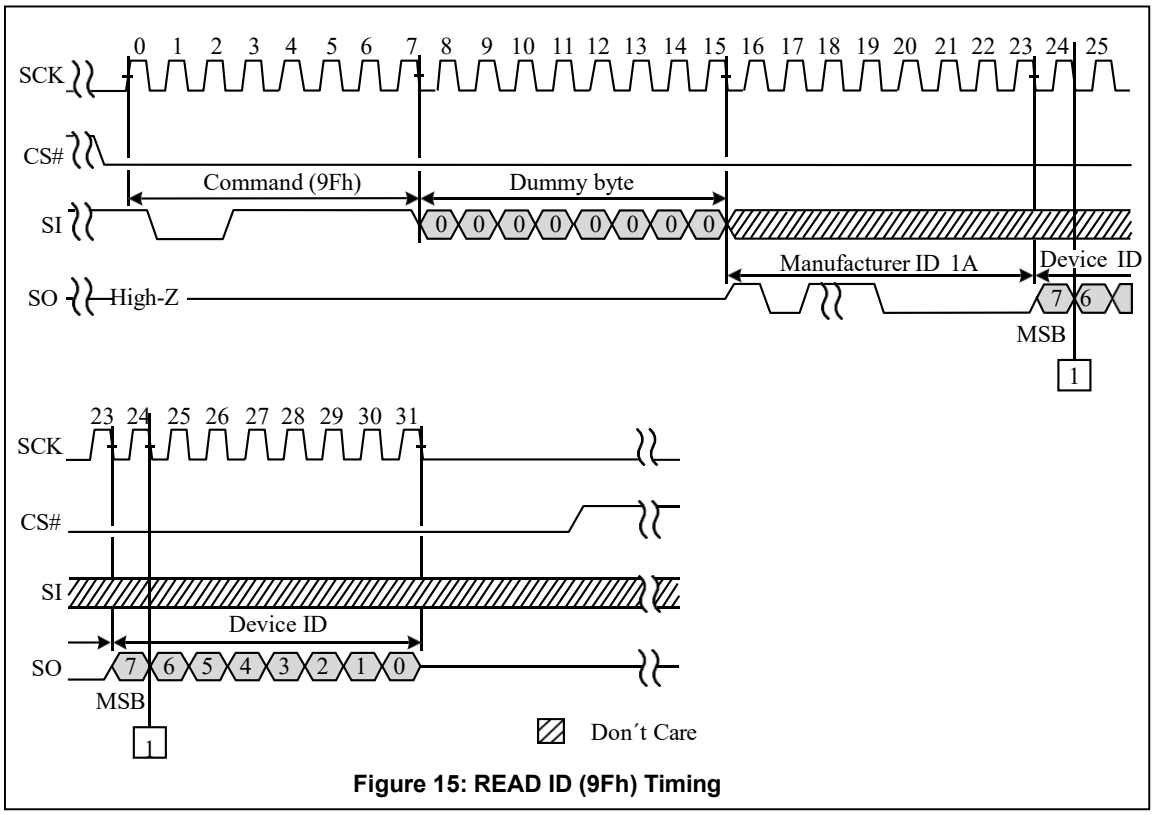


Figure 15: READ ID (9Fh) Timing

8.5.6 Parameter Page

The following command flow must be issued by the memory controller to access the parameter page contained within UniIC SPI devices:

- SET FEATURE (1Fh) command with feature address B0h and data value of 40h (Access to OTP/Parameter/UniqueID pages, ECC disable).
- PAGE READ (13h) command with block/page address of 0x01h, and then check the status of the read completion using the GET FEATURE (0Fh) command with feature address C0h.
- READ FROM CACHE (03h) command with an address of 0x00h to read the data out of the NAND device (refer to the following Parameter Page Data Structure table for a description of the contents of the parameter page).

Byte	Description	Value[1]
0-3	Parameter Page Signature	4Fh (O), 4Eh (N), 46h (F), 49h (I)
4-5	Revision number	00h, 00h
6-7	Feature Supported	00h, 00h
8-9	Optional Commands Supported 15-6: Reserved (0) 5: 1 = supports Read UniqueID 4: 1 = supports Copy back 3: 1 = supports Read Status Enhanced 2: 1 = supports Get Feature and Set Feature 1: 1 = supports Read Cache commands 0: 1 = supports Page Cache Program command	24h, 00h
10-31	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
32-43	Device Manufacturer	55h, 4Eh, 49h, 49h, 43h, 20h, 20h, 20h, 20h, 20h, 20h, 20h (UNIIC)
44-63	Device Model	53h, 43h, 46h, 31h, 41h, 57h, 31h, 49h, 33h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h; (**SCF1AW1I3A**) 53h, 43h, 46h, 31h, 41h, 57h, 32h, 49h, 33h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h; (**SCF1AW2I3A**) 53h, 43h, 46h, 31h, 41h, 57h, 31h, 43h, 32h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h; (**SCF1AW1C2A**) 53h, 43h, 46h, 31h, 41h, 57h, 32h, 43h, 32h, 41h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h, 20h; (**SCF1AW2C2A**)
64	Manufacture ID	1Ah
65-66	Date code	00h, 00h
67-79	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
80-83	Number of data bytes per page	00h, 08h, 00h, 00h
84-85	Number of spare bytes per page	40h, 00h
86-89	Number of data bytes per partial page	00h, 02h, 00h, 00h
90-91	Number of spare bytes per partial page	10h, 00h
92-95	Number of pages per block	40h, 00h, 00h, 00h

96-99	Number of blocks per unit	00h, 04h, 00h, 00h
100	Number of logical units	01h
101	Number of address cycles	00h
102	Number of bits per cell	01h

- To exit reading the parameter page, issue SET FEATURE (1Fh) command with feature address B0h and data value of 10h or 00h (main array READ, ECC enable/disable).

Table 8: Parameter Page Data Structure

103-104	Bad blocks maximum per unit	14h, 00h (1Gb)
105-106	Block endurance	06h, 04h (Byte 105 comprised the value; byte 106 comprised the multiplier; the calculation equation is value x $10^{multiplier}$
107	Guaranteed valid blocks at beginning of target	04h
108-109	Block endurance for guaranteed valid blocks	00h, 00h
110	Number of programs per page	04h
111	Partial programming attributes	00h
112	Number of ECC bits	00h
113	Number of interleaved address bits	00h
114	Interleaved operation attributes	00h
115-127	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
128	I/O Pin Capacitance	0Ah (pf)
129-130	Timing mode Support	00h, 00h (n/a)
131-132	Program Cache timing	00h, 00h (n/a)
133-134	tPROG maximum page program time	58h, 02h (600us)
135-136	tBERS maximum block erase time	10h, 27h (10000us)
137-138	tR maximum page read time	16h, 00h (22us)
139-163	Reserved	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
164-165	Vendor-specific revision number	00h, 00h (n/a)
166-253	Vendor specific	00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h, 00h
254-255	Integrity CRC	51h, 2Eh
256-511	Value of bytes 0-255	
511-767	Value of bytes 0-255	
768+	Additional redundant parameter pages	

Note: 1. h = hexadecimal.

8.5.7 UniqueID Page

The following command flow must be issued by the memory controller to access the uniqueID page contained within UnIIC SPI devices:

- SET FEATURE (1Fh) command with feature address B0h and data value of 40h (Access to OTP/Parameter/UniqueID pages, ECC disable).
- PAGE READ (13h) command with block/page address of 0x00h, and then check the status of the read completion using the GET FEATURE (0Fh) command with feature address C0h.
- READ FROM CACHE (03h) command with an address of 0x00h to read the data out of the NAND device. (The contents of the UniqueID page are described in the following note.)

  Note: The device stores 16 copies of the unique ID data. Each copy is 32 bytes; the first 16 bytes are unique data, and the second 16 bytes are the complement of the first 16 bytes. The host should XOR the first 16 bytes with the second 16 bytes. If the result is 16 bytes of FFh, then that copy of the unique ID data is correct. If a non-FFh result is returned, the host can repeat the XOR operation on a subsequent copy of the unique ID data.
- To exit reading the UniqueID page, issue SET FEATURE (1Fh) command with feature address B0h and data value of 10h or 00h (main array READ, ECC enable/disable).

8.6 Program Operations

8.6.1 PAGE PROGRAM

The PAGE PROGRAM operation sequence programs 1 byte to 2,112 bytes of data within a page. The page program sequence is as follows:

- 06h (WRITE ENABLE)
- 02h (PROGRAM LOAD)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing the PROGRAM LOAD operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE

must be executed in order to set the WEL bit. If this command is not issued, then the rest

of the program sequence is ignored. WRITE ENABLE must be followed by a PROGRAM LOAD (02h) command. PROGRAM LOAD consists of an 8-bit Op code, followed by 4 dummy bits, followed by a 12-bit column address, then the data bytes to be programmed. The data bytes are loaded into a cache register that is 2112 bytes long. Only four partial-page programs are allowed on a single page. If more than 2112 bytes are loaded, then those additional bytes are ignored by the cache register. The command sequence ends when CS# goes from LOW to HIGH.

After the data is loaded, a PROGRAM EXECUTE (10h) command must be issued to initiate the transfer of data from the cache register to the main array. PROGRAM EXECUTE consists of an 8-bit Op code, followed by a 24-bit address (8 dummy bits and a 16-bit page/block address for 1Gb). After the page/block address is registered, the memory device starts the

transfer from the cache register to the main array, and is busy for tPROG time. During this busy time, the status register can be polled to monitor the status of the operation. When the operation completes successfully, the next series of data can be loaded with the PROGRAM LOAD command.

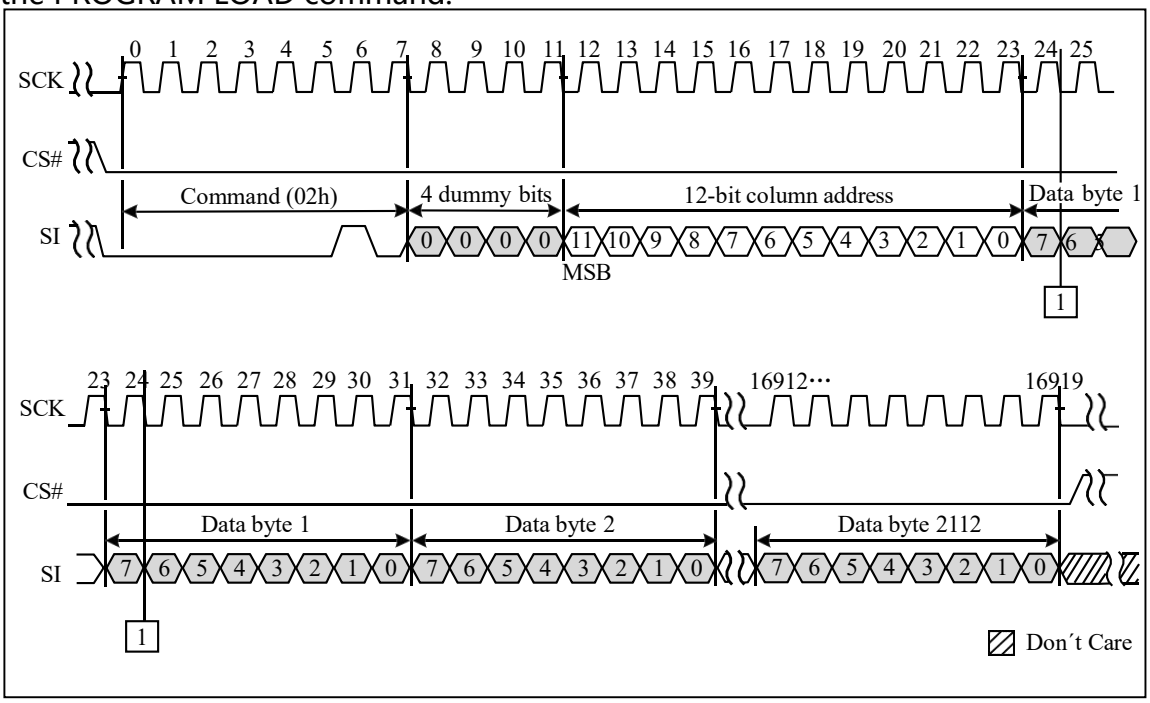


Figure 16: PROGRAM LOAD (02h) Timing

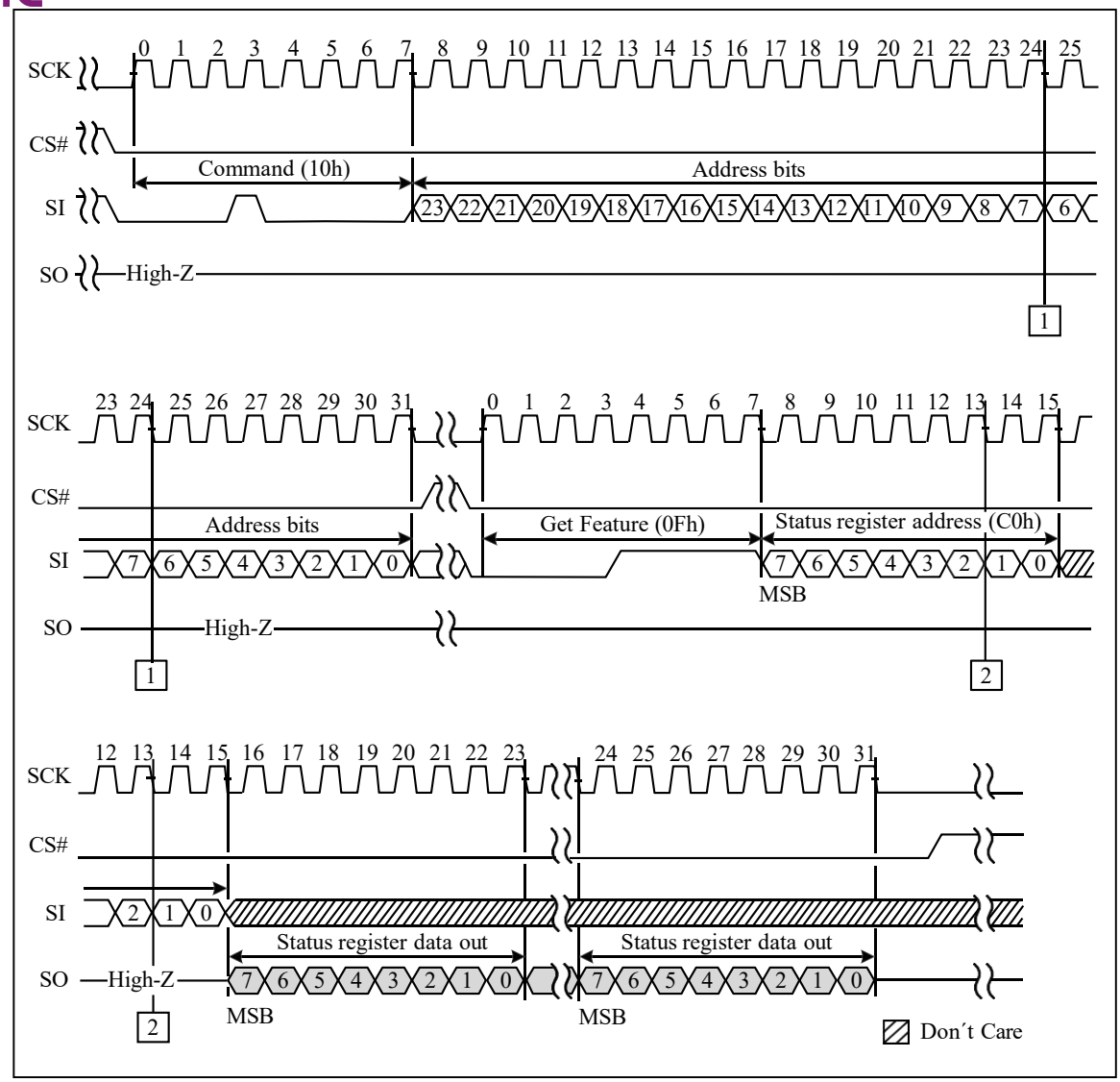


Figure 17: PROGRAM EXECUTE (10h) Timing

8.6.2 RANDOM DATA PROGRAM

The RANDOM DATA PROGRAM sequence programs or replaces data in a page with existing data. The random data program sequence is as follows:

- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing a PROGRAM LOAD RANDOM DATA operation, a WRITE ENABLE (06h) command must be issued to change the contents of the memory array. Following a WRITE ENABLE (06) command, a PROGRAM LOAD RANDOM DATA (84h) command must be issued. This command consists of an 8-bit Op code, followed by 4 dummy bits, followed by a 12-bit column address. New data is loaded in the column address provided with the 12 bits. If the random data is not sequential, then another PROGRAM LOAD RANDOM DATA (84h) command must be issued with a new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation.

Both PROGRAM LOAD x1 and PROGRAM LOAD RANDOM DATA x1 instructions are the same command sequence. The difference is that PROGRAM LOAD x1 instruction will reset the cache buffer to all FFh value, while PROGRAM LOAD RANDOM DATA x1 instruction will only update the data bytes that are specified by the command input sequence and the rest of data in the cache buffer will remain unchanged.

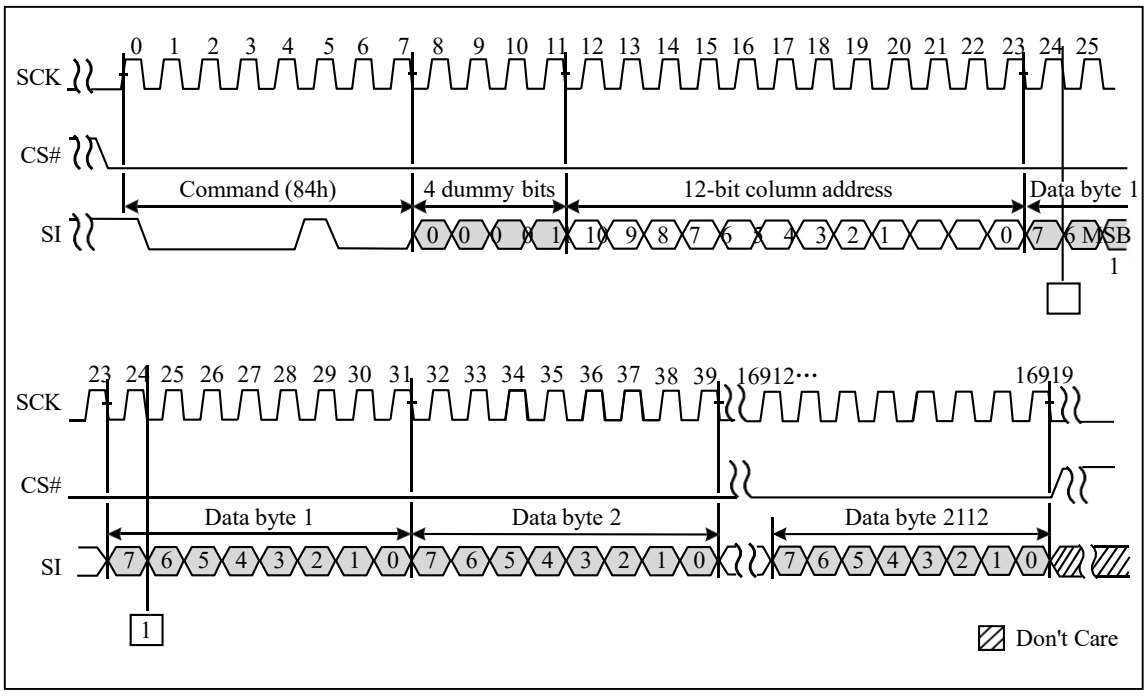


Figure 18: PROGRAM LOAD RANDOM DATA (84h) Timing

8.6.3 PROGRAM LOAD x4 (32h) / PROGRAM LOAD RANDOM DATA x4 (34h)

The PROGRAM LOAD x4 and PROGRAM LOAD RANDOM DATA x4 instructions are enigmatical to the PROGRAM LOAD and PROGRAM LOAD RANDOM DATA in terms of operation sequence and functionality. The only difference is that x4 instructions will input the data bytes from all four IO pins instead of the single SI pin. This method will significantly shorten the data input time when a large amount of data needs to be loaded into the cache buffer.

Both PROGRAM LOAD x4 and PROGRAM LOAD RANDOM DATA x4 instructions are the same command sequence. The difference is that PROGRAM LOAD x4 instruction will reset the cache buffer to all FFh value, while PROGRAM LOAD RANDOM DATA x4 instruction will only update the data bytes that are specified by the command input sequence and the rest of data in the cache buffer will remain unchanged.

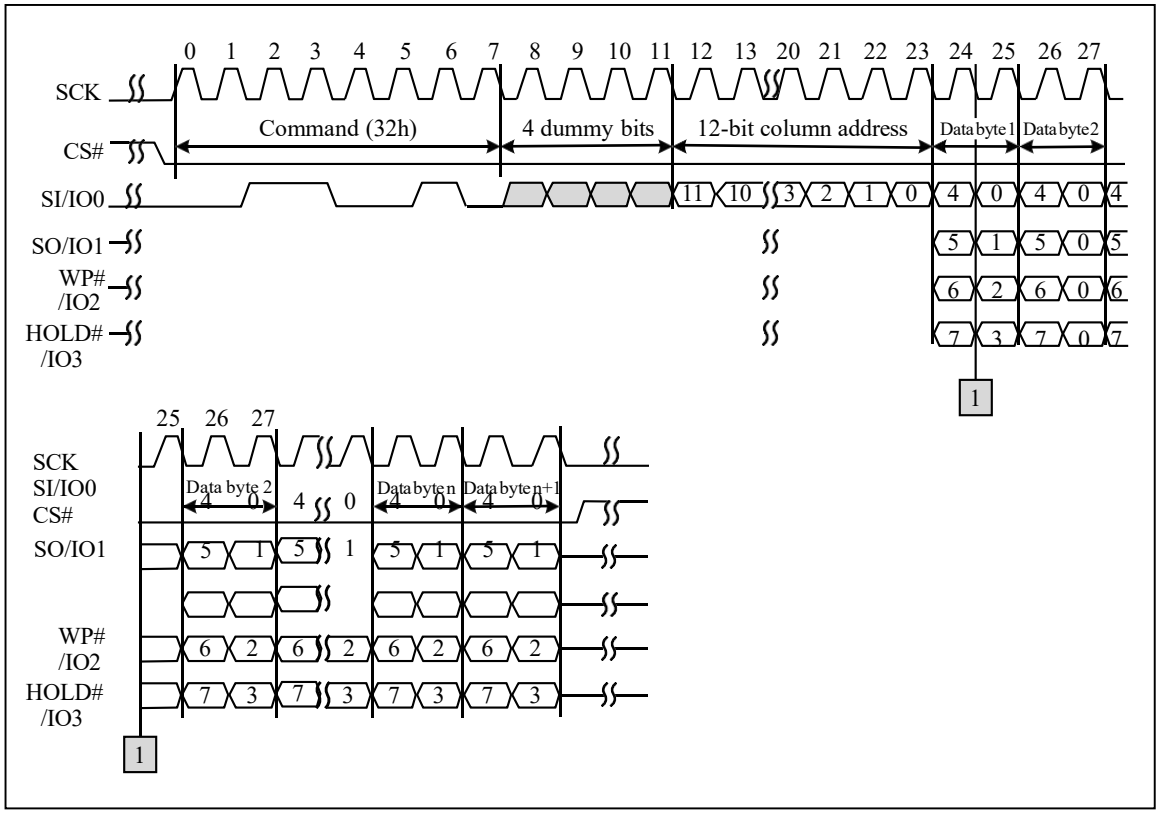


Figure 19: PROGRAM LOAD x4 (32h) Timing

8.6.4 INTERNAL DATA MOVE

The INTERNAL DATA MOVE command sequence programs or replaces data in a page with existing data. The INTERNAL DATA MOVE command sequence is as follows:

- 13h (PAGE READ to cache register)
- 06h (WRITE ENABLE)
- 84h (PROGRAM LOAD RANDOM DATA) or 34h (PROGRAM LOAD RANDOM DATA x4)
- 10h (PROGRAM EXECUTE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing an internal data move operation, the target page content must be read into the cache register. This is done by issuing a PAGE READ (13h) command. The

PAGE READ command must be followed with a WRITE ENABLE (06h) command in order

to change the contents of memory array. After the WRITE ENABLE command is issued, the PROGRAM LOAD RANDOM DATA (84h) command or PROGRAM LOAD RANDOM
DATA x4 (34h) can be issued. This command consists of an 8-bit Op code, followed by 4 dummy bits, followed by a 12-bit column address. New data is loaded in the 12-bit column address. If the random data is not sequential, another PROGRAM LOAD RANDOM DATA (84h) command or PROGRAM LOAD RANDOM DATA x4 (34h) must be issued with the new column address. After the data is loaded, a PROGRAM EXECUTE (10h) command can be issued to start the programming operation. It is not possible to use the INTERNAL DATA MOVE operation to move data from one die (LUN) to another.

8.7 BLOCK ERASE (D8h)

The BLOCK ERASE (D8h) command is used to erase at the block level. The blocks are organized as 64 pages per block, 2112 bytes per page (2048 + 64 bytes). Each block is 132 Kbytes. The BLOCK ERASE command (D8h) operates on one block at a time. The command sequence for the BLOCK ERASE operation is as follows:

- 06h (WRITE ENABLE)
- D8h (BLOCK ERASE)
- 0Fh (GET FEATURE command to read the status)

Prior to performing the BLOCK ERASE operation, a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE command must be executed in order to set the WEL bit. If the WRITE ENABLE command is not issued, then the rest of the erase sequence is ignored. A WRITE ENABLE command must be followed by a BLOCK ERASE (D8h) command. This command requires a 24-bit address consisting of 8 dummy bits followed by a 16-bit page/block address for 1Gb. After the row address is registered, the control logic automatically controls timing and erase-verify operations. The device is busy for tERS time during the BLOCK ERASE operation. The GET FEATURE (0Fh) command can be used to monitor the status of the operation.

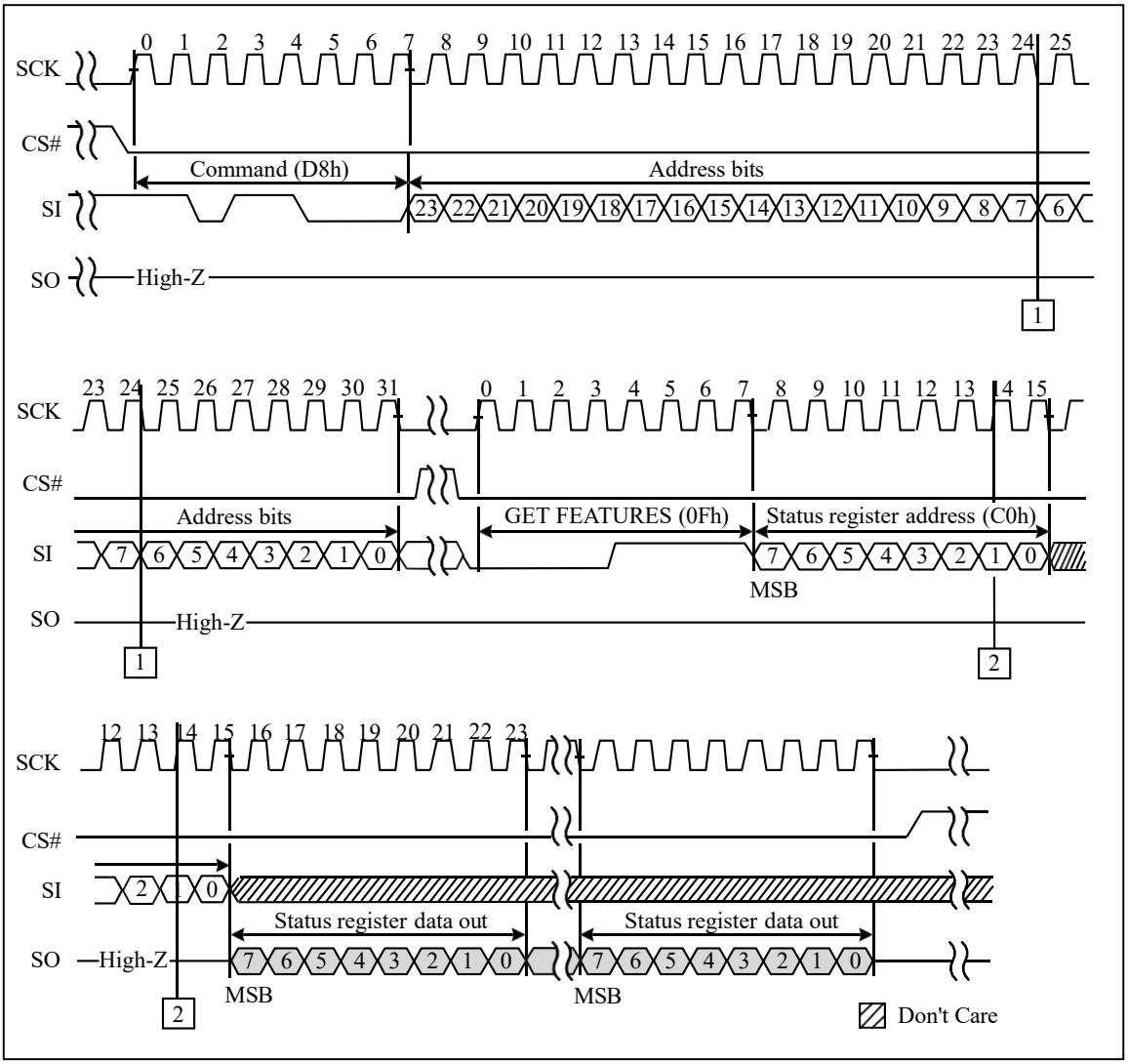


Figure 20: BLOCK ERASE (D8h) Timing

8.8 Block Lock Feature

The block lock feature protects either the entire device or ranges of blocks from being programmed or erased.

Before the contents of the device can be modified, the device must first be unlocked. Either a range of blocks or the entire device may be unlocked. PROGRAM and ERASE operations complete successfully only in the block ranges that have been unlocked. Blocks, once unlocked, can be locked again to protect them from further PROGRAM and Erase operations.

Also blocks that are locked can be protected further or locked tight. When locked tight, the device's blocks can no longer be locked or unlocked unless next power cycle.

But once the blocks are locked through Protect command, these blocks would be permanently protected from PROGRAM or ERASE operations.

The following diagram shows block lock scheme in this product.

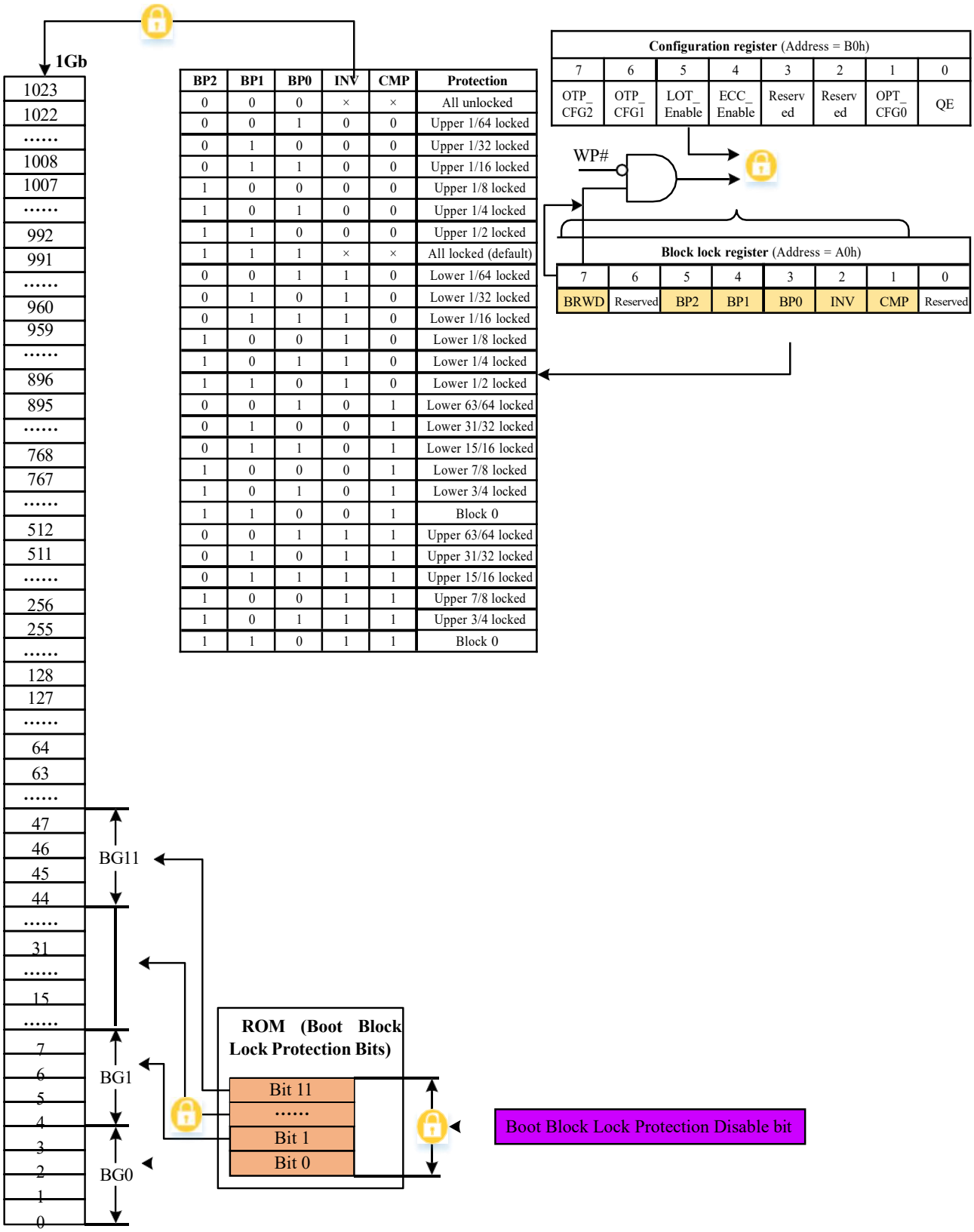


Figure 21: Block Lock Scheme (1Gb)

8.8.1 Block Lock

The block lock feature provides the ability to protect the entire device, or ranges of blocks, from the PROGRAM and ERASE operations. After power-up, the device is in the locked state, i.e., bits 1, 2, 3, 4, and 5 of the block lock register are set to 1. To unlock all the blocks, or lock a range of blocks, the SET FEATURE command must be issued with feature address A0h and data value of the block protection bits shown in Table 9. When BRWD is set and WP# is LOW, none of the writable bits (1, 2, 3, 4, 5 and 7) in the block lock register can be changed. Also, when a PROGRAM/ERASE command is issued to a locked block, a status to indicate operation failure is returned. When an ERASE command is issued to a locked block, the erase failure, 04h, is returned. When a PROGRAM command is issued to a locked block, program failure, 08h, is returned.

Table 9: Block Lock Register Block Protection Bits

Block Protection Bits					Protected Portion
BP2	BP1	BP0	INV	CMP	
0	0	0	x	x	All unlocked
0	0	1	0	0	Upper 1/64 locked
0	1	0	0	0	Upper 1/32 locked
0	1	1	0	0	Upper 1/16 locked
1	0	0	0	0	Upper 1/8 locked
1	0	1	0	0	Upper 1/4 locked
1	1	0	0	0	Upper 1/2 locked
1	1	1	x	x	All locked (default)
0	0	1	1	0	Lower 1/64 locked
0	1	0	1	0	Lower 1/32 locked
0	1	1	1	0	Lower 1/16 locked
1	0	0	1	0	Lower 1/8 locked
1	0	1	1	0	Lower 1/4 locked
1	1	0	1	0	Lower 1/2 locked
0	0	1	0	1	Lower 63/64 locked
0	1	0	0	1	Lower 31/32 locked
0	1	1	0	1	Lower 15/16 locked
1	0	0	0	1	Lower 7/8 locked
1	0	1	0	1	Lower 3/4 locked
1	1	0	0	1	Block 0
0	0	1	1	1	Upper 63/64 locked
0	1	0	1	1	Upper 31/32 locked
0	1	1	1	1	Upper 15/16 locked
1	0	0	1	1	Upper 7/8 locked
1	0	1	1	1	Upper 3/4 locked
1	1	0	1	1	Block 0

For example, if all the blocks need to be unlocked after device initialization, the following sequence should be performed:

- Issue SET FEATURE command (1Fh)
- Issue the feature address to unlock the block (A0h)
- Issue 00h on data bits to unlock all blocks

8.8.2 LOCK TIGHT

Lock Tight prevents locked blocks from being unlocked and also prevents unlocked blocks from being locked. Once Lock Tight is enabled, this mode cannot be disabled via a software command and BP bits, INV and CMP bit and BRWD is protected from further software change. Only another power down and power up cycle could disable Lock Tight. The command sequence to enable LOCK TIGHT is as follows:

- Issue SET FEATURE command (1h)
- Issue the feature address to configuration register bits (B0h)
- Issue 20h on data bits to enable lock tight

During Quad mode, this could provide software protection to prevent locked/unlocked blocks from change if WP# is disabled.

8.8.3 PROTECT Command (PERMANENT BLOCK LOCK PROTECTION 2Ch)

The PROTECT command provides nonvolatile, irreversible protection of up to twelve groups (48 blocks total, also named as boot blocks) shown in Figure 21, "Block Lock Scheme (1Gb)" on page 31.

Implementation of the protection is group-based, which means that a minimum of one group (4 blocks) is protected when the PROTECT command is issued. Because block protection is nonvolatile, a power-on or power-off sequence does not affect the block status after the PROTECT command is issued. The device ships from the factory with no blocks protected so that users can program or erase the blocks before issuing the PROTECT command. Block protection is also irreversible in that when protection is enabled by the issuing PROTECT command, the protected blocks can no longer be programmed or erased. If Boot block lock protection disable mode is enabled, PROTECT command would be ignored and has no busy time.

The PROTECT sequence is as detailed below:

- 06h (WRITE ENABLE)
- 2Ch (Permanent Block Lock Protection)
- 0Fh (GET FEATURE command to read the status)

Prior to performing the Protection command (2Ch), a WRITE ENABLE (06h) command must be issued. As with any command that changes the memory contents, the WRITE ENABLE must be executed in order to set the WEL bit. If this command is not issued, then

the protection command is ignored. WRITE ENABLE must be followed by a Protection command (2Ch). The Protection command consists of an 8-bit Op code, followed by a 24- bit address (8 dummy bits and a 16-bit page/block address for 1Gb).

After the page/block address is registered, the corresponding boot block lock protection bit would be programmed to lock corresponding boot block group. This operation is shown in Figure 22, "Protection Command (2Ch) Timing" on page 34. During this busy time, the status register can be polled to monitor the status of the operation. P_FAIL bit = 0 indicates the success of protection operation; P_FAIL bit = 1 indicates the failure of protection operation.

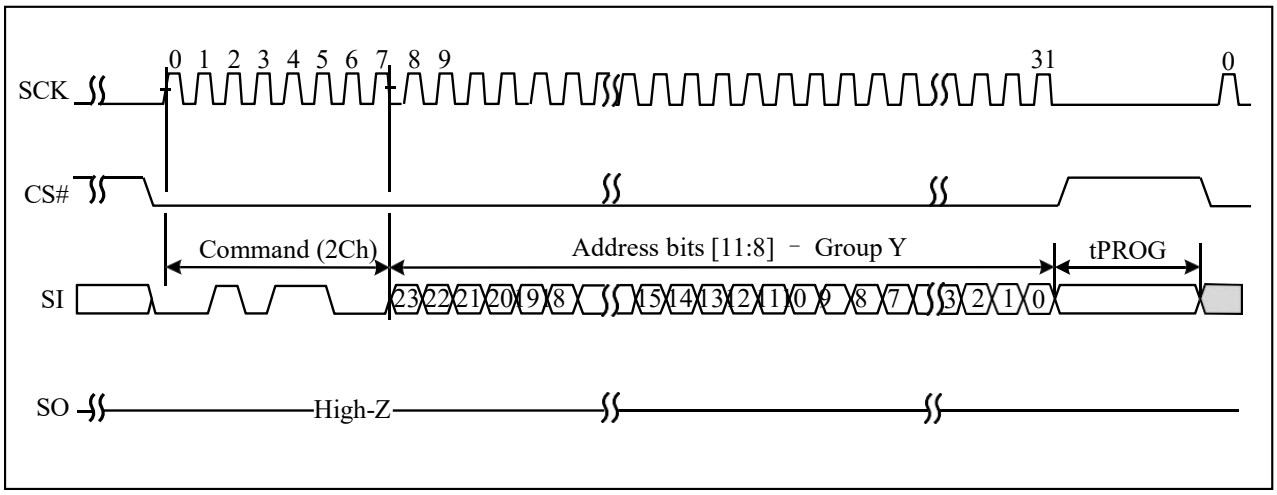


Figure 22: Protection Command (2Ch) Timing

8.8.3.1 PROTECTION Command Details

To enable protection, the Protection command consists of an 8-bit Op code, followed by a 24-bit address (8 dummy bits and a 16-bit page/block address for 1Gb). Row address bits 8, 9, 10, 11 (named as Y, bit 12~15 must be kept as '0') input the targeted block group information.

This Y defines the group of blocks to be protected. There are always 12 Groups, so Y = 0000b - 1011b:

- Y = 0000 protects Group0 = blks 0, 1, 2, 3
- Y = 0001 protects Group1 = blks 4, 5, 6, 7
- Y = ...
- Y = 1011 protects Group11 = blks 44, 45, 46, 47

After tPROG, the targeted block groups are protected. Upon PROTECT operation failure, the status register reports a value of 08h (P_FAIL = 1). Upon PROTECT operation success, the status register reports value of 00h.

8.9 OTP Feature

The serial device offers a protected, one-time programmable (OTP) NAND Flash memory area. Ten full pages (2112 bytes per page) are available on the device, and the entire range is guaranteed to be good.

Customers can use the OTP area any way they want; typical uses include programming serial numbers, or other data, for permanent storage.

The OTP area leaves the factory in an erased state (all bits are 1). Programming an OTP page changes bits that are 1 to 0, but cannot change bits that are 0 to 1. The OTP area cannot be erased, even if it is not protected. Protecting the OTP area prevents further programming of the pages in the OTP area.

To access the OTP feature, the user must issue the SET FEATURE command, followed by feature address B0h. When the OTP is ready for access, pages 02h-0Bh can be programmed in sequential order. The PROGRAM LOAD (02h) and PROGRAM EXECUTE (10h) commands can be used to program the pages. Also, the PAGE READ (13h) command can be used to read the OTP area. The data bits used in feature address B0h to enable OTP access are shown in the Table 10, "OTP Configuration States" on page 35.

8.9.1 OTP Access Configuration

To access OTP, perform the following command sequence:

- Issue the SET FEATURE command (1Fh)
- Issue the configuration feature address (B0h)
- Issue the PAGE PROGRAM or PAGE READ command

For OTP states, see the following table.

Table 10: OTP Configuration States

OTP_CFG2	OTP_CFG1	OTP_CFG0	State
0	0	0	Normal Operation
0	1	0	Access OTP area / Parameter page / UniqueID (named as OTP Operation Mode)
1	0	0	Normal Operation (Reserved)
1	1	0	Access to OTP Data Protection bit to lock OTP area (named as OTP DATA protection mode)
0	0	1	Normal Operation (Reserved)
0	1	1	Normal Operation (Reserved)
1	0	1	Normal Operation (Reserved)
1	1	1	Access to Disable Boot Block Lock Protection (named as Boot block lock protection disable mode)

8.9.2 OTP Area Access

The OTP area is accessible while the OTP operation mode is enabled. To enable OTP operation mode, issue the SET FEATURE (1Fh) command to feature address B0h and data value of 40h (OTP operation mode and ECC disable) or 50h (OTP operation mode and ECC enable).

When the die is in OTP operation mode, all subsequent PAGE PROGRAM or PAGE READ commands are applied to the OTP area. Erase commands are not valid while the device is in OTP operation mode.

Each page in the OTP area is programming using the PAGE PROGRAM sequence described at Section 8.6.1, "PAGE PROGRAM" on page 23. Each page can be programmed more than once up to the maximum number allowed. By reading the P_FAIL bit of the status register, program operation passed or failed could be determined. If the host attempts to program the OTP pages which are out of bounds, program command will be ignored and P_FAIL bit = 1 will be reported. If the host attempts to program the OTP pages after OTP area is protected, the program command will be ignored and P_FAIL bit is set to '1' indicating program failure.

To read pages in the OTP area, whether the OTP area is protected or not, issue the PAGE READ command sequence described at Sction 8.5.1, "PAGE READ" on page 16. If the host issues the PAGE READ (13h) command to an address beyond maximum page-address range, the data output will not be valid. To determine whether the device is busy during an OTP operation, use GET FEATURE command at feature address C0h to check OIP bit.

To exit from OTP operation mode and return to normal array operation mode, issue the SET FEATURE (1Fh) command with feature address B0h and data value of 00h or 10h.

If the RESET (FFh) command is issued while in OTP operation mode, the device will exit OTP operation mode and enter normal operation mode.

Note: In OTP operation mode, page address 00h is to read out UniqueID page; page address 01h is to read out parameter page.

8.9.3 OTP DATA PROTECT

OTP DATA PROTECT mode is used to prevent further programming of pages in the OTP area. In OTP DATA PROTECT mode, the following program sequence is used to enable OTP DATA protect:

- SET FEATURE (1Fh) command with feature address B0h and data value of C0h (access OTP DATA PROTECT mode)
- WRITE ENABLE (06h)
- PROGRAM EXECUTE (10h) command with block/page address all '0'
- GET FEATURE (0Fh) command with status register address C0h to check the device is ready or busy (OIP bit)

When the device is ready, check the P_FAIL bit of the status register to determine if the operation passed or failed.

If the program sequence is issued again after the OTP area has already been protected, program command will be ignored, the status register is set to 00h.

8.9.4 OTP Configuration to Disable Protection Command

Boot block lock protection disable mode is used to prevent further adding non-volatile locked block groups by protection command. In Boot block lock protection disable mode, the following program sequence is used to disable protection command to add more non- volatile locked block groups:

- SET FEATURE (1Fh) command with feature address B0h and data value of C2h (access Boot Block lock protection disable mode)
- WRITE ENABLE (06h)
- PROGRAM EXECUTE (10h) command with block/page address all '0'
-

GET FEATURE (0Fh) command with status register address C0h to check the device is ready or busy (OIP bit)

When the device is ready, check the P_FAIL bit of the status register to determine if the operation passed or failed.

If the program sequence is issued again after boot block lock protection is disabled, program command will be ignored and the status register is set to 00h.

8.10 Status Register

The SPI NAND Flash device has an 8-bit status register that software can read during the device operation. The status register can be read by issuing the GET FEATURE (0Fh) command, followed by the feature address C0h.

The status register will output the status of the operation. The descriptions of data bits from status register are shown in the following table.

Table 11: Status Register Bit Descriptions

it	Bit Name	Description
SR[0] (OIP)	Operation in progress	This bit is set (OIP = 1) when a PROGRAM EXECUTE, PAGE READ, BLOCK ERASE, PROTECTION or RESET command is executing; the device is busy. When the bit is 0, the interface is in the ready state.
SR[1] (WEL)	Write Enable Latch	This bit indicates the current status of the write enable latch (WEL) and must be set (WEL = 1), prior to issuing a PROGRAM EXECUTE or BLOCK ERASE command. It is set by issuing the WRITE ENABLE command. WEL can also be disabled (WEL = 0), by issuing the WRITE DISABLE command or successful program/erase operation.
SR[2] (E_Fail)	Erase fail	This bit indicates that an erase failure has occurred (E_Fail set to 1). This bit will also be set if the user attempts to erase a locked region, or if the ERASE operation fails. This bit is cleared (E_Fail = 0) at the start of the BLOCK ERASE command sequence or the RESET command.
SR[3] (P_Fail)	Program fail	This bit indicates that a program failure has occurred (P_Fail set to 1). This bit will also be set if the user attempts to program an invalid address or a locked or protected region, including the OTP area. This bit is cleared during the PROGRAM EXECUTE command sequence or a RESET command (P_Fail = 0).
SR[6:4] (ECCS2, ECCS1, ECCS0)	ECC Status Register	ECC_Status provides ECC status as follows: 000b = No bit errors detected during the previous read algorithm. 001b = Bit errors detected and corrected; no data refreshment is required. 010b = Bit errors detected and not corrected. 011b = Bit errors detected and corrected; data refreshment is recommended 100b = Reserved 101b = Bit errors detected and corrected; data refreshment is mandatory. 110b = Reserved 111b = Invalid state ECC_Status is set to 000b either following a RESET or at the beginning of PAGE READ. It is then updated after the device completes a valid READ operation. ECC_Status is invalid if ECC is disabled (via a SET FEATURE command to B0h address). After power-up RESET or device initialization, ECC status is set to reflect the contents of block 0, page 0.
SR[7]	Reserved	

8.11 Error Management

This NAND Flash device is specified to have the minimum number of valid blocks (NVB) of the total available blocks per die shown in Table 12. This means the devices may have blocks that are invalid when shipped from the factory. An invalid block is one that contains at least one page that has more error bits than can be corrected by the minimum required ECC. Although NAND Flash device may contain invalid blocks, the valid blocks of the device are of the same quality and reliability with reference to AC and DC characteristicsas. Internal circuitry isolates each block from other blocks, so the presence of a invalid block does not affect the operation of the rest of the NAND Flash array. NAND Flash devices are shipped from the factory erased. The factory identifies invalid blocks before shipping by attempting to program the bad-block mark in the first and second page of each invalid block. The first spare area location in each bad block is guaranteed to contain the bad-block mark.

Table 12: Error Management Details

Description	Requirement
Minimum number of valid block (NVB)	1004
Total available blocks per die	1024
First spare area location	Byte 2048th
Bad-block mark	00h

System software should initially check the first spare area location for non-FFh data on the first or second page of each block prior to performing any program or erase operations on the NAND Flash device, refer to Figure 23. A bad-block table can then be created, enabling system software to map around these areas. Note that it may not be possible to recover the bad-block marking if the block is erased.

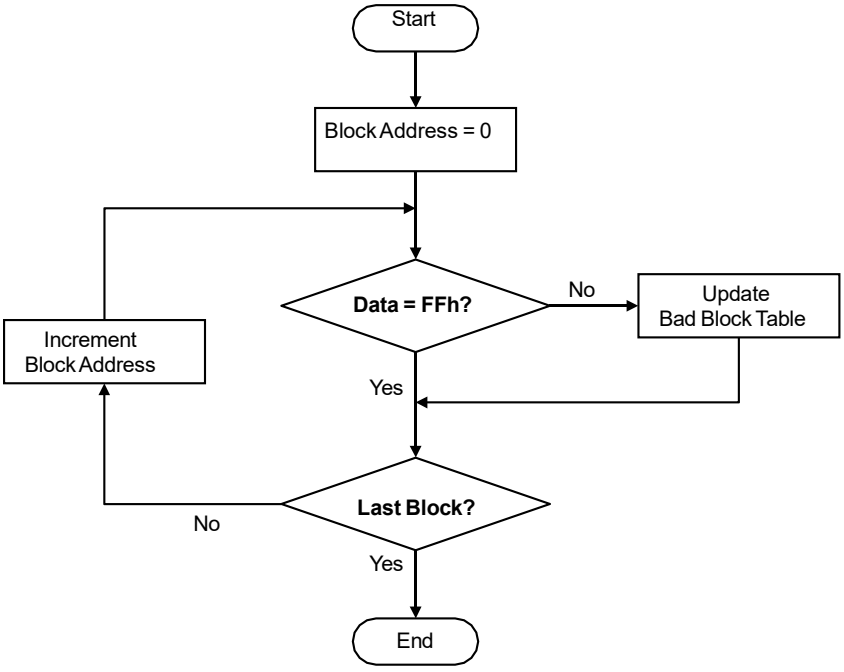


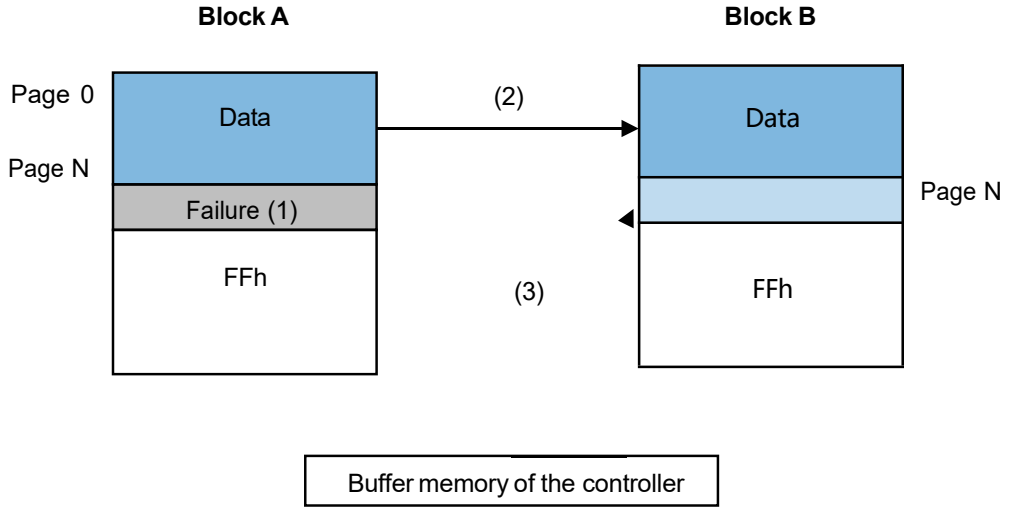
Figure 23: Bad Block Management Flowchart

Additional bad blocks may develop with use over the lifetime. In this case, each bad block has to be replaced by copying any valid data to a new block. These addtional bad blocks can be identified by checking ECCS2,1,0, P_Fail and E_Fail bit in the Status Register, after each read, program and erase operation.

The failure of a page program operation does not affect the data in other pages in the same block, thus the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block.

Table 13: Block Failure

Operation	Detection	Recommended procedure
Erase	Status register read after erase, check E_Fail bit	Block replacement
Program	Status register read after program, check P_Fail bit	Block replacement
Read	Status register read, check ECCS2,1,0 bit	ECC correction



Note:

1. An error occurs on page N of Block A during a program operation.
2. Data in page 0 to N-1 of Block A is copied to the same location of Block B which is a valid block.
3. Data in page N of Block A which is in controller buffer memory is copied into the page N of Block B.
4. Update bad block table to prevent from erasing or programming Block A.

Figure 24: Bad Block Replacement

8.12 ECC Protection

The serial device offers data corruption protection by offering 8-bit internal ECC at least. READs and PROGRAMs with internal ECC can be enabled or disabled by setting the ECC bit in the configuration register. ECC is enabled after device power up, so the default READ and PROGRAM commands operate with internal ECC in the active state. To enable/disable ECC, perform the following command sequence:

- Issue the SET FEATURE command (1Fh).
- Issue the OTP feature address (B0h).
- Then:

· Set bit4 (ECC_ENABLE) to 1, to enable ECC

· Clear bit4 (ECC_ENABLE) to 0, to disable ECC

During a PROGRAM operation, the device calculates an ECC code on the 2KB page in the cache register, before the page is written into the NAND Flash array. The ECC code is stored in the extra hidden spare area of the page.

During a READ operation, the page data is read from the array to the cache register, where the ECC code is calculated and compared with the ECC code value read from the array. If a bit error is detected and corrected, only corrected data is output on the I/O bus. The ECC status bit indicates whether or not the error correction was successful shown as Table 15, "ECC Status" on page 42. The ECC Protection table shown Table 14, "ECC Protection" on page 42 below shows the ECC protection scheme used throughout a page.

With internal ECC, the user must accommodate the following:

- Spare area definitions provided in the ECC Protection table shown Table 14, "ECC Protection" on page 42.
- ECC protected are supported for main and spare areas 0, 1, 2 and 3. The "Main 0" and "Spare 0" are belonging to one ECC sector, and the same for main and spare 1, 2, 3.
- When using partial-page programming, the following conditions must both be met:

· In the main user area and in user spare area, single partial-page programming operations must be used.

· Within a page, the user can perform a maximum of four partial-page programming operations.

Note: If ecc feature is off, ecc status should be ignored and user needs to clear ecc status by issuing RESET command after ecc off.

Table 14: ECC Protection

Max Byte Address	Min Byte Address	ECC Protected	Area	Description
1FFh	000h	Yes	Main 0	User data 0
3FFh	200h	Yes	Main 1	User data 1
5FFh	400h	Yes	Main 2	User data 2
7FFh	600h	Yes	Main 3	User data 3
80Fh	800h	Yes	Spare 0	Spare 0
81Fh	810h	Yes	Spare 1	Spare 1
82Fh	820h	Yes	Spare 2	Spare 2
83Fh	830h	Yes	Spare 3	Spare 3

Table 15: ECC Status

Bit 2	Bit 1	Bit 0	Description
0	0	0	No bit errors detected during the previous read algorithm
0	0	1	Bit errors detected and corrected; no data refreshment is required.[1]
0	1	0	Bit errors detected and not corrected
0	1	1	Bit errors detected and corrected; data refreshment is recommended.[1]
1	0	0	Reserved
1	0	1	Bit errors detected and corrected; data refreshment is required.[1]
1	1	0	Reserved
1	1	1	Invalid state

Note: 1. bit0 = 1 indicates bit errors/sector were detected and corrected.

9. Electrical Characteristics

9.1 Maximum Rating

Stressing the device outside the ratings listed here may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this datasheet, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 16: Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
T_{STG}	Storage temperature		–65	150	°C
V_{CC}	Supply voltage	1.8V	–0.6	2.4	V
V_{IN}	Voltage Applied to Any Pin	1.8V	–0.6	2.4	V

9.2 Power Up / Power Down

9.2.1 SPI Power Up

UNIIC NAND Flash devices are designed to prevent data corruption during power transitions. V_{CC} is internally monitored and when V_{CC} reaches 1.5V @1.8V, the device automatically performs the device initialization within tPUW and also performs power-on read. The first page data would be automatically loaded into cache register. The first access to the SPI NAND device can occur at tPUW (2ms) after V_{CC} reaches V_{CC} min and then CS# can be driven LOW, SCK can start, and the required command can be issued to the SPI NAND device. Note that CS# must track the V_{CC} supply level during power up until V_{CC} reaches V_{CC} min. If needed a pull-up resistor on CS# can be used to accomplish this.

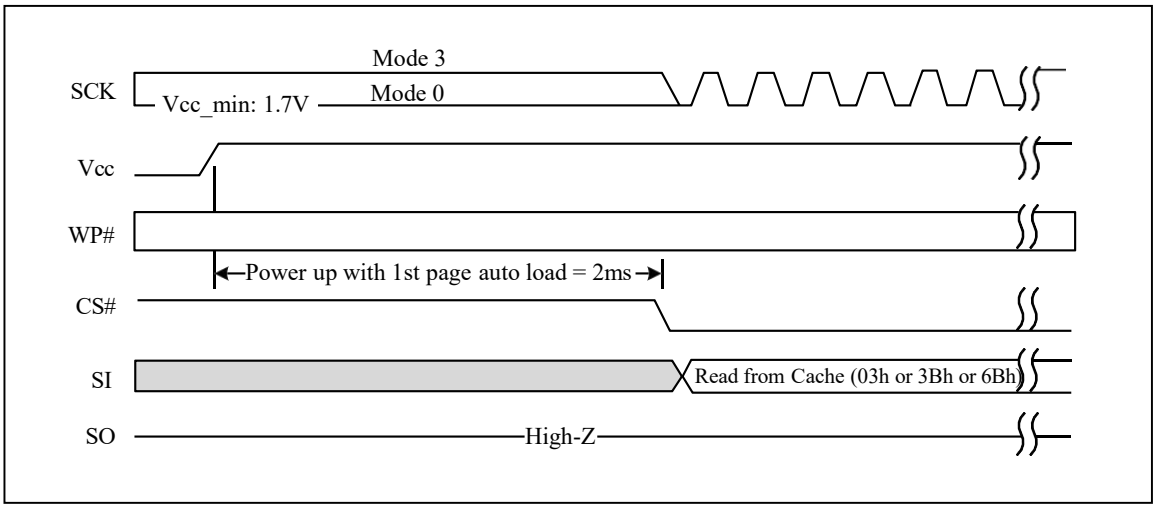


Figure 25: Automatically Device Initialization after Power is ready

9.2.2 SPI Power Down

Upon power-down the NAND device requires a maximum voltage and minimum time that the host should hold V_{CC} below the voltage prior to power on. Note that CS# must also track the V_{CC} supply level during power down to prevent adverse command sequence.

Table 17: Power-down Maximum Voltage and Minimum Time

Parameter	Value	Unit
Maximum V_{CC}	100	mV
Minimum time below maximum voltage	100	ns

Note: the target V_{CC} slew rates for 1.8V: 1mV/us < ramp rate < 50mV/us

9.3 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 18: Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply voltage	1.7	1.8	1.95	V
V_{SS}	Ground Supply voltage	0	0	0	V
T_A	Ambient operating temperature	-20	25	70	°C

Table 19: AC measurement Conditions

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	15 / 10		pF
	Input rise and fall times[1]	-	5	ns
	Input rise and fall times (for >=80MHz)[2]	-	2.1	ns
	Input rise and fall times (for >=100Mhz)[2]	-	1.5	ns
	Input timing reference voltages	$0.3V_{CC}$ to $0.7V_{CC}$		V
	Output timing reference voltages	V_{CC} / 2		V

Note: 1. Applicable to 20Mhz or 66MHZ

2. 20% of clock period

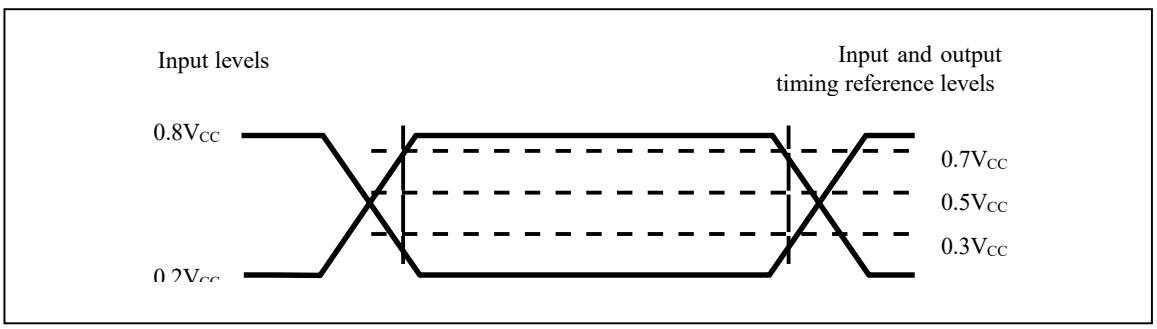


Figure 26: AC measurement I/O Waveform

Note: 1. For Dual and Quad operations rail-to-rail assumed for input levels

Table 20: Capacitance

Symbol	Parameter	Test condition	Min	Max	Unit
$C_{IN/OUT}$	Input/output capacitance ($IO_0/IO_1/IO_2/IO_3$)	V_{OUT} = 0 V	–	8	pF
C_{IN}	Input capacitance (other pins)	V_{IN} = 0 V	–	6	pF

Note: Sampled only, not 100% tested, at T_A=25° C and a frequency of 54MHz.

Table 21: DC Characteristics[1]

Symbol	Parameter	Test condition	Min	Typ	Max	Unit
I_{LI}	Input leakage current	V_{IN} = 0V to V_{CC}	–	–	±10	µA
I_{LO}	Output leakage current	V_{OUT} = 0V to V_{CC}	–	–	±10	µA
ICC1(2)	Standby current, 1.8V V_{CC}	CS# = V_{CC}, V_{IN} = V_{SS} or V_{CC}	–	10	50	µA
ICC2(3)	Sequential Read current, 1.8V V_{CC} (x1 IO)	SCK = 0.1V_{CC} / 0.9V_{CC} at 104MHz, SO = open		–	14	mA
	Sequential Read current, 1.8V V_{CC} (x2 IO)	SCK = 0.1V_{CC} / 0.9V_{CC} at 104MHz		–	16	mA
	Sequential Read current, 1.8V V_{CC} (x4 IO)	SCK = 0.1V_{CC} / 0.9V_{CC} at 104MHz		–	18	mA
ICC3(4)	Page Read current	CS# = V_{CC}	–	10	20	mA
ICC4(5)	Program current	CS# = V_{CC}	–	10	20	mA
ICC5	Erase current	CS# = V_{CC}	–	7.5	15	mA
ICC6(6)	Power-up current		–	–	10	mA
V_{IL}(7)	Input low voltage		– 0.5	–	0.3V_{CC}	V
V_{IH}(7)	Input high voltage		0.7V_{CC}	–	V_{CC}+0.4	V
V_{OL}	Output low voltage	I_{OL} = 1.6 mA	–	–	0.4	V
V_{OH}	Output high voltage	I_{OH} = –100 µA	V_{CC}–0.2	–	–	V

Note:

1. All currents are RMS unless noted. Typical values at typical V_{CC} (1.8V), V_{IO}=0V/V_{CC}, T_C=25° C
2. Standby current is the average current measured over any 5ms time interval 5us after CS# de-assertion (and any internal operations are completed).
3. All read currents are average current measured over any 2KB continuous reads. No Load, checker board pattern.
4. All Page read currents are average current measured over any one page read checker board pattern.
5. All program currents are average current measured over any 2KB typical data program.
6. Measurement is taken over 1.25ms with interval 5us and begins after V_{CC} reaches V_{CC} min
7. V_{IL} can undershoot to –1.0V for periods <2ns and V_{IH} may overshoot to V_{CC} (max)+1.0V for periods less than 2ns.

Table 22: AC Characteristics

Symbol	Alt.	Parameter	Min	Typ1	Max	Unit
fC	fC	Clock frequency for the all the instructions (including Extended-SPI protocol)	D.C.	–	104	MHz
tCH(2)	tWH	Clock High time	4.3	–	–	ns
tCL(2)	tWL	Clock Low time	4.3	–	–	ns
tCLCH(3)	tCRT	Clock rise time (peak to peak) 1.8V VCC	0.7	–	–	V/ns
tCHCL(3)	tCFT	Clock fall time (peak to peak) 1.8V VCC	0.7	–	–	V/ns
tSLCH	tCSS	CS# active setup time (relative to SCK)	4.3	–	–	ns
tSHCH		CS# not active setup time (relative to SCK)				
tCHSH	tCSH	CS# active hold time (relative to SCK)	3	–	–	ns
tCHSL		CS# not active hold time (relative to SCK)				
tDVCH	tSUDAT	Data in setup time	4	–	–	ns
tCHDX	tHDDAT	Data in hold time	2	–	–	ns
tSHSL	tCS	Command deselect time	50	–	–	ns
tSHQZ(3)	tDIS	Output disable time	–	–	15	ns
tCLQV	tV	Clock Low to Output valid under 15 pF	–	–	8	ns
		Clock Low to Output valid under 10 pF	–	–	7	ns
tCLQX	tHO	Output hold time under 30pF	2.5	–	–	ns
		Output hold time under 10pF	2	–	–	ns
tHLCH	tHD	HOLD# setup time (relative to SCK)	4.3	–	–	ns
tCHHH	tCD	HOLD# non-active hold time (relative to SCK)	4.3	–	–	ns
tHHCH	tHC	HOLD# non-active setup time (relative to SCK)	4.3	–	–	ns
tCHHL	tCH	HOLD# hold time (relative to SCK)	4.3	–	–	ns
tHHQX(3)	tLZ	HOLD# High to Output Low-Z	–	–	15	ns
tHLQZ(3)	tHZ	HOLD# Low to Output High-Z	–	–	15	ns
tWHSL	tWPS	WP# setup time	20	–	–	ns
tSHWL	tWPH	WP# hold time	100	–	–	ns

Note:

1. Typical values given for T_A=25° C.
2. tCH + tCL must add up to 1/fC; 45% - 55% duty cycle is considered.
3. Value guaranteed by characterization, not 100% tested in production.

Table 23: Program/Erase Characteristics

Symbol	Parameter	Typ	Max	Unit
NOP(1)	Number of partial-page programming operations	–	4	Cycles
tPROG(2)	Page Program Time (ECC Disabled)	350	600	us
	Page Program Time (ECC Enabled)	400	600	
tRD	Data Transfer Time from NAND Flash array to data Register with internal ECC Disabled	–	22	us
	Data Transfer Time from NAND Flash array to data Register with internal ECC Enabled	–	95	
tERS	BLOCK ERASE operation Time	3	10	ms
tRST	Resetting time for Read/Program/Erase	–	10/15/300	us
tPOR	Power-on reset time (device initialization)	–	2	ms

Note:

1. Four total partial-page programs to the same page. If ECC is enabled, the device is limited to one partial-page program per ECC user area, not exceeding four partial-page programs per page.
2. This cover protection command execution time also.

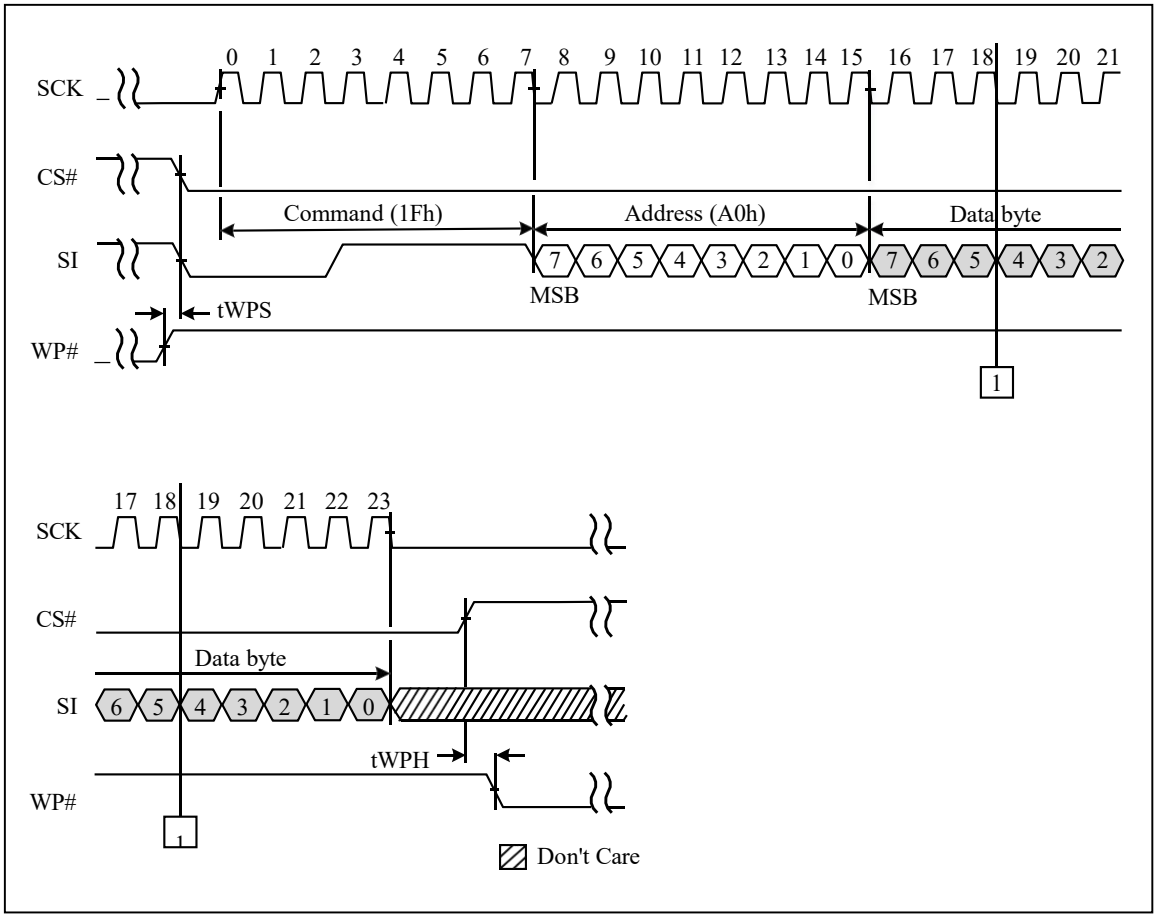


Figure 27: WP# Timing

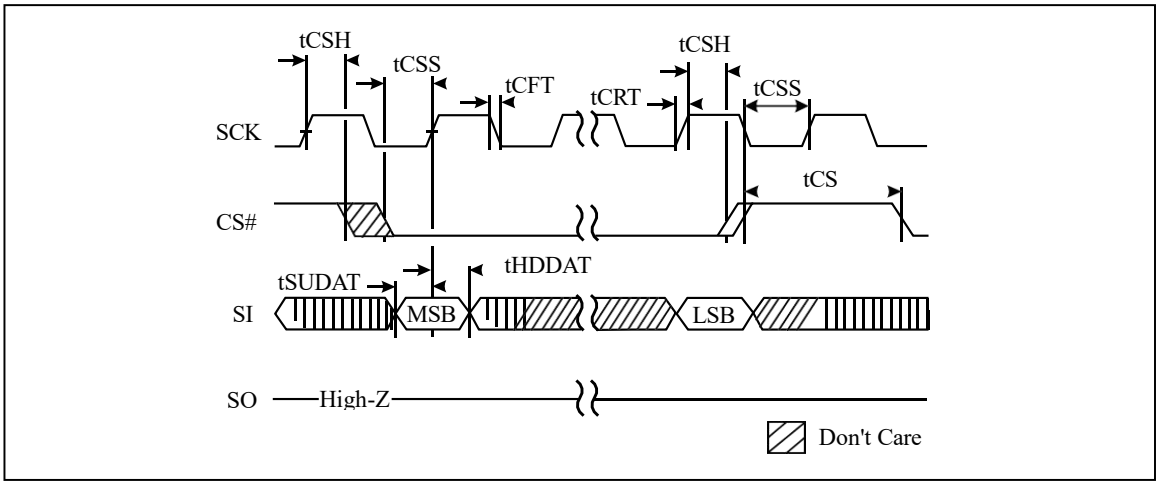


Figure 28: Serial Input Timing

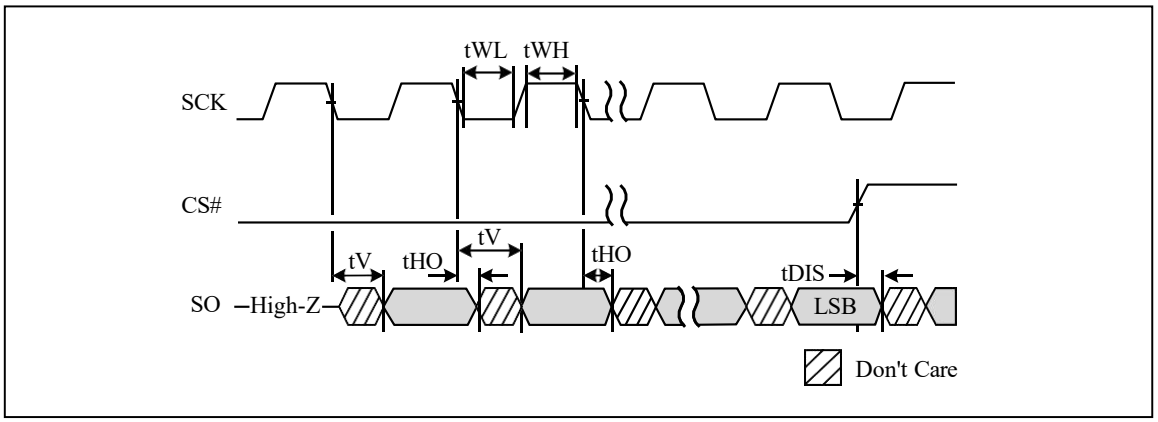


Figure 29: Serial Output Timing

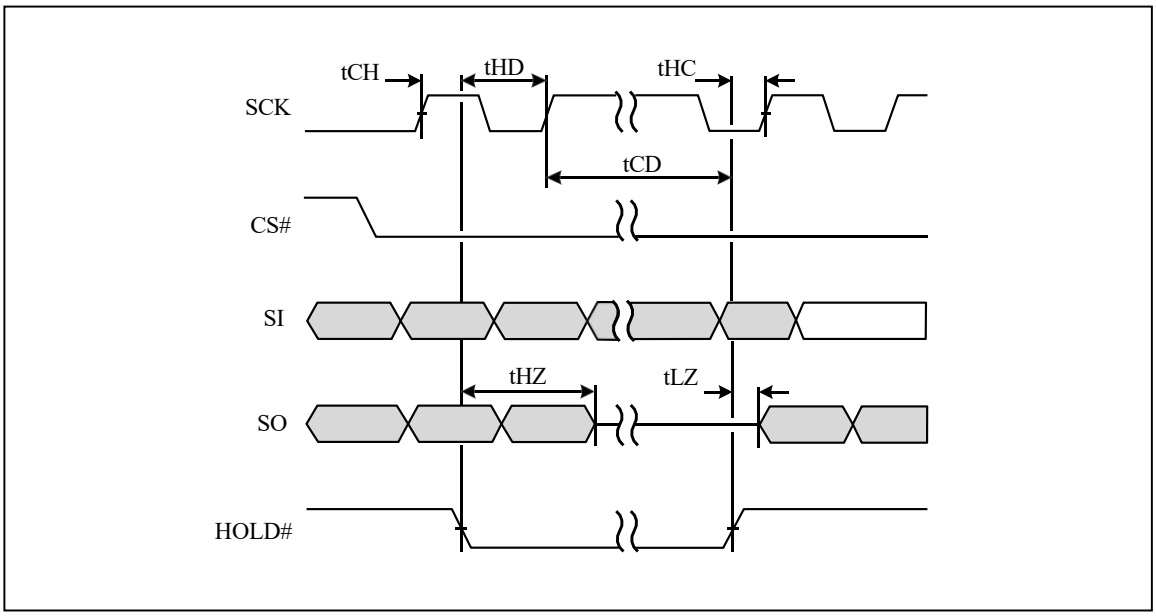
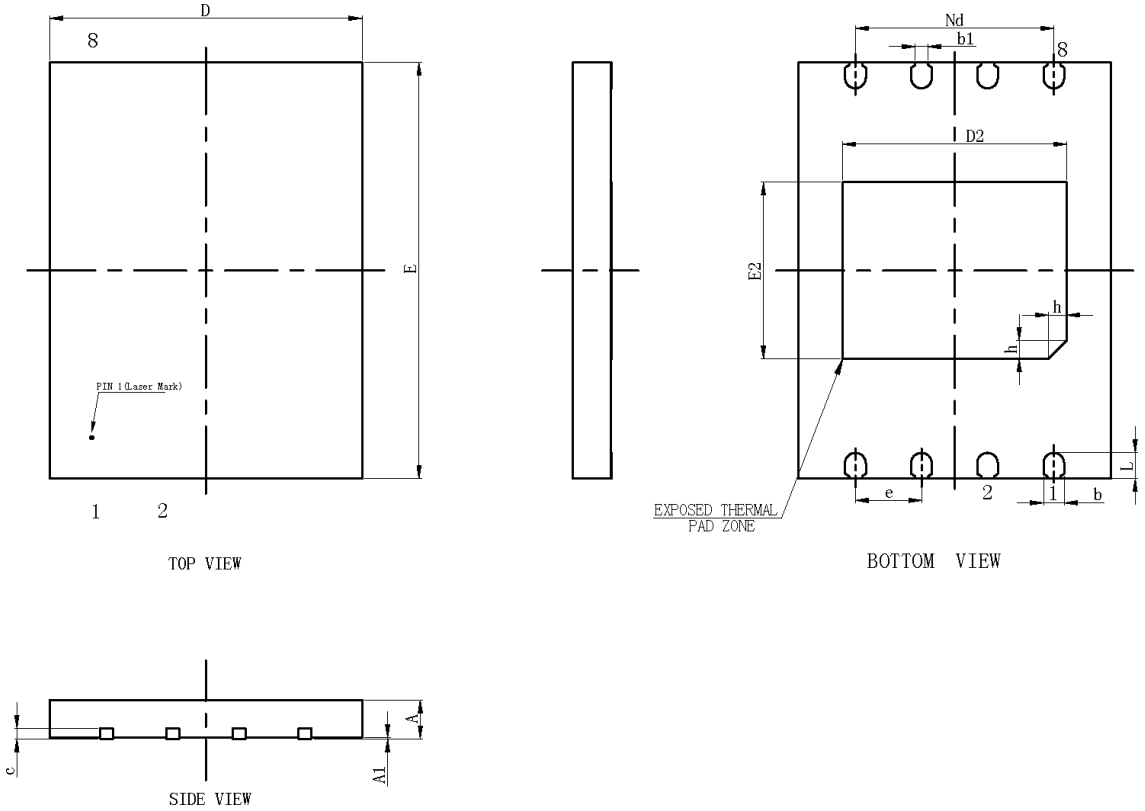


Figure 30: Hold# Timing

10. Package diagram



Symbol	Millmeter		
	Min	Nom	Max
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.35	0.40	0.45
b1		0.25 (ref.)	
c	0.18	0.203	0.25
D	5.90	6.00	6.10
Nd		3.81 (basic)	
e		1.27 (basic)	
E	7.90	8.00	8.10
D2	4.20	4.30	4.40
E2	3.30	3.40	3.50
L	0.45	0.50	0.55
h	0.30	0.35	0.40

Figure 31: Package Diagram and Dimension of WSON8 (8mm x 6mm)

Edition 2024-12
Published by
Xi'an UniIC Semiconductors Co., Ltd.

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